DIGITAL STORAGE AND REALTIME OSCILLOSCOPE OS1400

Instruction Manual

GOULD

MP MASTER
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Introduction

Section 1

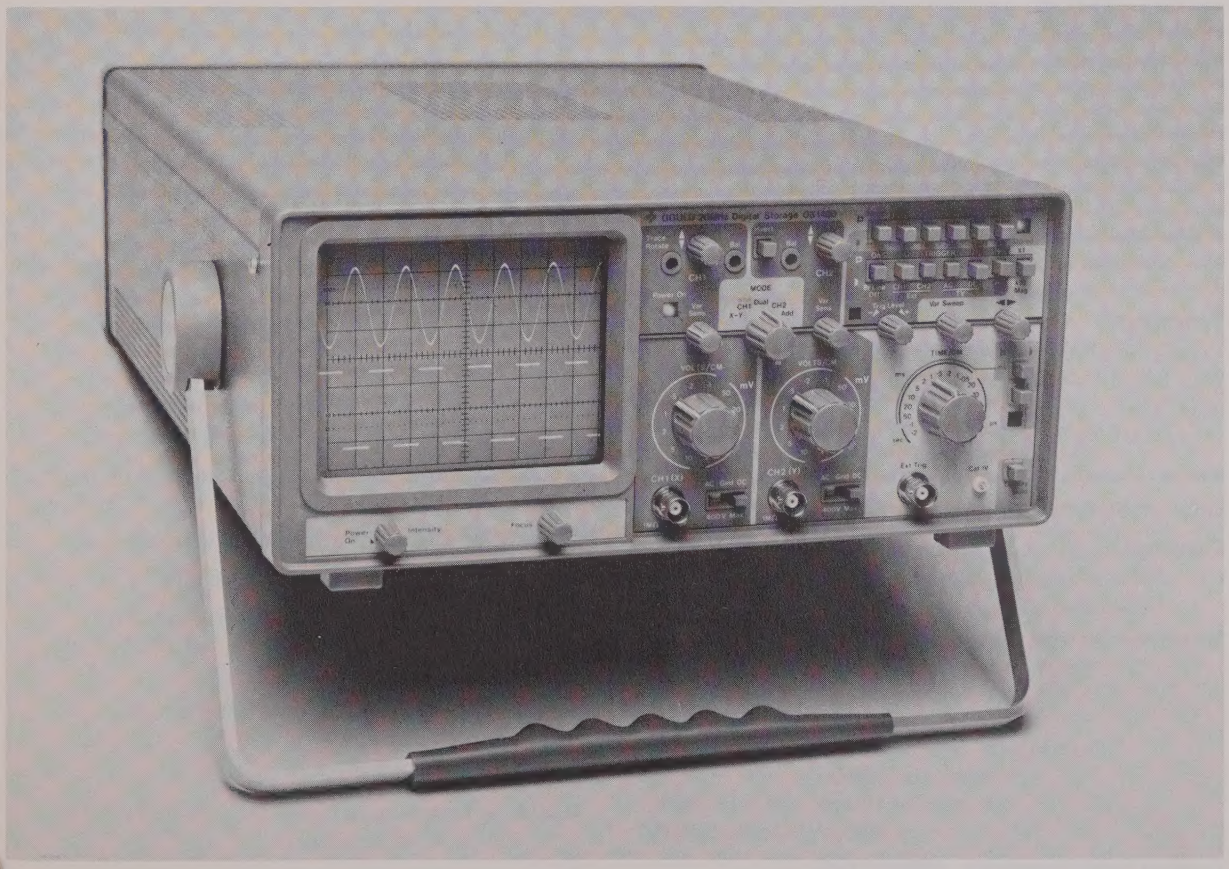
The Gould OS1400 provides a combination of Digital Storage and Real-time facilities, and caters for measurements from DC to 20MHz with a flicker-free display of a full cycle down to 0.002Hz. The digital method of storage provides many advantages, notably the facilities for pretrigger viewing and the ability to store a waveform indefinitely.

It features two identical input channels with a maximum sensitivity of 2mV/cm and a bandwidth from DC up to 20MHz. The channels may be displayed separately or together in both STORE and the conventional NORMAL modes. The ability to display the sum or difference of the channels and an X-Y mode operation are available in NORMAL mode. The timebase ranges from 0.5μs/cm to 0.25s/cm in NORMAL mode and 0.25ms/cm to 50s/cm in STORE mode. A x 10 facility expands the upper limit to 50ns/cm in NORMAL mode. In NORMAL and certain of the STORE modes, independent variable sensitivity and separate controls are provided.

The trigger facilities available are comprehensive, with DC and AC coupling available and a bright-line-free run facility to enable true location in the absence of a trigger. An active TV sync. separator is provided for viewing video waveforms.

Additional facilities are provided with the OS1400 such as a 1kHz calibrator, a DC coupled Z modulation input and a trace rotation control.

The instrument is readily portable and the use of an uncommitted logic array has reduced both the number of components and board area. This has additional benefits in terms of reliability, power consumption and ease of maintenance.



DISPLAY

CRT 8 x 10cm rectangular mono-accelerator

EHT 2kV (Trace rotation by front panel preset).

VERTICAL DEFLECTION

Two identical input channels CH1 and CH2.

Bandwidth –3db
d.c. to 20MHz (2Hz to 20MHz on a.c.)

Sensitivity 2mV/cm to 10V/cm in 1–2–5 sequence.

Accuracy ±3%.

Variable Sensitivity >2–5:1 range allows continuous adjustment of sensitivity 2mV/cm to 25V/cm.

Input Impedance: 1MΩ/28pF.

Input Coupling DC–GND–AC.

Input Protection 400V d.c. or pk a.c.

HORIZONTAL DEFLECTION

Normal Mode Sweep Rate 0.5μs/cm to 0.2sec/cm, 18 ranges in 1–2–5 sequence

Accuracy ±3% (to 200ns/cm).

Variable Sweep >2.5:1 allows continuous coverage from 0.5μs/cm to 0.5sec/cm.

Store Modes Sweep Rate 0.05ms/cm to 50 sec/cm, 25 ranges in 1–2–5 sequence.

Accuracy ±3% (to 200ns/cm).

Variable Sweep >2.5:1 allows continuous coverage from 0.5μs/cm to 50μs/cm (sampling only).

X Expansion X10 push button gives fastest speed of 50ns/cm in NORMAL. Accuracy ±3% (50ns ±5%).

TRIGGER

Variable level control with Bright Line ON/OFF facility. With Bright Line on, the timebase free-runs when insufficient signal (20Hz to 20MHz) is present or when the selected level is outside the range of the input signal.

Source Internal CH1 or CH2 External.

Slope Positive or negative.

Coupling DC, AC or TV (active sync separator with line/frame selected by timebase switch between 50 and 100μs/cm).

Sensitivity Internal: DC coupled 2mm to 2MHz, 1mm to 20MHz.
AC coupled 2mm, 10Hz – 2MHz.
1mm, 4Hz – 20MHz.
External: DC coupled 100mV to 2MHz, 400mV to 20MHz.
AC coupled 100mV, 10Hz to 2MHz.
400mV, 4Hz to 20MHz.

External Input Impedance 100kΩ/10pF.

External Input Protection 250V d.c. or pk a.c.

DISPLAY MODES

Single trace CH1 or CH2. (in Store CH1 only)

Dual trace In Normal, Chopped or Alternate Modes automatically selected by the timebase switch. Between 0.5μs/cm and 0.2ms/cm the Alternate Mode is selected whilst on ranges slower than 0.2ms/cm Chop Mode is selected. The chop frequency is 500kHz. (NORMAL Mode only) (In store modes simultaneous capture).

Add CH1 and CH2 added to give the algebraic sum of the two channel inputs (Normal mode only).

Invert CH2 CH2 may be inverted. When used in conjunction with Add mode it gives the algebraic difference of the two channels.

X–Y CH1 input gives X deflection and CH2 input gives Y deflection. (Normal mode only).

ADDITIONAL FACILITIES

Calibrator 1V ±2% square wave at approx. 1kHz.

Z Mod Input DC coupled, 2V visible mod.
Sensitivity +40V cut off sensitivity.
Input impedance 10kΩ/10pF approx.
Maximum input 100V d.c. or pk a.c.

DIGITAL FACILITIES

Store Size 1024 x 8-bits

Vertical Resolution 1 in 256 approx. 30 steps/cm.

Horizontal Resolution 1 in 1024 approx. 100 samples/cm. (0.05ms/cm range on Dual is 50 samples/cm).

Expansion X10 reduces the resolution by ten on all ranges.

Sample Rate: 2MHz (0.5μs) reducing in proportion with timebase.

Dot Joining Linear interpolation between samples.

DISPLAY MODES

Roll Stored data and display updated continually. (timebase ranges 50sec/cm to 0,05ms/cm).

Refreshed Stored data and display updated by triggered sweep. (timebase ranges 50sec/cm to 0.05ms/cm).

Single Shot Freezes store at end of triggered sweep.

Display Hold Freezes store immediately.

Pretrigger Storage Available in Roll mode only, switchable fro 0%, 25%, 75% and 100% of full store pre-trigger.

Supply 100V, 120V, 220V and 240V ±10%. 45 to 400Hz, 40VA approx.

Safety Designed for IEC 348 Cat 1.

Operating Temperature Range 0 to 50°C (+15°C to 35°C for full accuracy).

Dimensions 140 x 305 x 460mm. (5.5") x (12.0") x (18.1")

Weight 6kg approx.

Accessories Supplied Handbook PN 450770.
Mains Lead PN 402001

Optional Accessories

Probe Kit PB12
A passive probe kit with switched X1 and X10 attenuators .
X10 attenuation input impedance is 10MΩ/11.5pF.

Probe Kit PB13
A X10 passive probe with 1.5m of cable. Input impedance 10m/11.5pF.

Probe Kit PB17
A X100 passive probe with 1.5m of cable.
Input impedance 100MΩ//4.5pF.
Working voltage 1.5kV inc pk a.c.

Viewing Hood PN450401
Front Panel Cover PN450240
Rack Mount Kit PN450070

Trolley Type TR7 General Purpose

Protective Carrying Case PN42610 – A strong case which completely encloses the oscilloscope with 3 thicknesses of padded material covering the front panel.

INTERNATIONAL SAFETY WARNING
(as required for I.E.C. 348 Class I)

This instruction manual contains information and warnings which must be observed by the user to ensure safe operation and retain the apparatus in a safe condition. The instrument has been designed for indoor use within the specified limits of temperature. It should not be switched on if there are obvious signs of mechanical damage and it should not be used under wet conditions.

EARTHING
The instrument must be operated with a protective earth connected via the appropriate (yellow/green) conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply socket is inserted into the plug on the back of the instrument. If the final connection between the instrument and the supply is made elsewhere, the user must ensure earth connection is made before line and neutral.

If any supply cable other than that supplied with the instrument is used, it must carry an adequate protective earth conductor.

Any interruption of the protective earth conductor inside or outside the instrument is likely to make the instrument dangerous. Intentional interruption is prohibited.

Signal connections into the instrument should be connected after and disconnected before the protective earth connection is made, i.e. the supply lead must be connected at all times that signal leads are connected.

LIVE PARTS
The instrument is safe to operate with the covers fitted and these must not be removed under normal usage. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance or repair purposes. (see maintenance section).

VENTILATION
The OS1400 relies on convection cooling and must not be operated in a position which restricts the external circulation of air.

3.1 CONNECTION TO THE SUPPLY

1. Before connecting the OS1400 to the supply, check that the supply range switches are set to suit the supply voltage to be used and that the correct fuse is fitted. Note that the fuse has to be changed when switching between the 100V and 220V ranges. The switches and fuse holder are mounted on the back panel of the instrument. Do not operate the range selection switches while the OS1420 is switched on.

3.2 OBTAINING A TRACE

1. After connection to the supply, switch on by turning the INTENSITY control clockwise away from the OFF position. Check that the POWER indicator l.e.d. lights.
2. Set the:
   Set NORM/STORE switch to NORM.
   MODE switch to CH1.
   CH1 Y shift control (vert. arrows) to approx. mid setting.
   CH1 VAR SENS control fully clockwise to the CAL position.
   CH1 input coupling switch to GND.
   BRIGHT LINE button out (ON).
   X MAG. button out (X1).
   X shift control (horiz. arrows) to approx mid setting.
   TIME/CM switch to 5μs.
   A horizontal trace should appear on the screen as the INTENSITY control is advanced.
3. Adjust the INTENSITY control to obtain a display of the required brightness.
4. Adjust the FOCUS control to obtain a sharply defined trace.
5. Adjust the CH1 Y shift control and the X shift control to centralise the trace on the screen.
6. Adjust the TRACE ROTATE preset control if necessary to align the trace with the centre graticule line. It may be necessary to re-adjust this control only when the instrument is re-positioned as the beam deflection can be affected by Earth's magnetic field or other sources of magnetic radiation.

NOTE: The OS1400 should not be operated close to sources of alternating magnetic field such as large transformers as these may interfere with the trace.

3.3 SETTING UP THE Y CHANNELS

1. Using a coaxial input signal lead, connect a signal to the CH1 or CH2 input socket.
2. For
   (a) Direct connection of the input signal, set the associated AC–Ground–DC slide switch to DC.
   (b) Capacitative coupling of the input signal through an internal 0.1μF 400V capacitor, set the slide switch to AC.

NOTE: When examining low amplitude a.c. signals superimposed on a high d.c. level, the slide switch should be set to AC and the sensitivity of the Y amplifier increased as in (4).

3. To locate the base line, set the slide switch to the GND setting. At this setting, the input signal is open circuit and the input to the amplifier is connected to ground.

4. To select sensitivity, set the VOLTS/CM switch to the required range. For calibrated operation, the VARiable SENsitivity control should be set fully clockwise to the CAL position. This control can be used however to reduce the gain of the relevant amplifier and obtain any intermediate sensitivity between the calibrated switched ranges. To set to any particular calibrated sensitivity, the actual variation from the calibrated range can be set by viewing the CAL 1 Volt o/p on the 0.1V/cm or 0.2V/cm ranges. If the VAR SENS control is not moved, the sensitivity will differ from the calibrated value by approximately the same proportion on all settings of the VOLTS/CM switch.

   To minimise pick-up at sensitive settings, it is essential to ensure that the ground lead connection is near to the signal point.

5. For vertical movement of the trace, adjust the Y shift controls (identified by the vertical arrows).

6. Any trace movement under no-signal conditions, when the setting of the VOLTS/DIV switch is altered, can be overcome by adjustment of the relevant preset front panel balance control.

   This control will only need adjustment at infrequent intervals. Before adjusting the BAL control, however, ensure that the input coupling switch is set to GND.

   No adjustment should be made until a minimum of 15 min. warm-up time has elapsed after switch-on, or immediately after any large change of ambient temperature.

3.4 DISPLAY MODES

The mode switch determines the form of the display. In the STORE mode some of the display modes are not available. These will be indicated in the relevant paragraph.

3.4.1 SINGLE CHANNEL

For single trace display of one Y input against the timebase this switch should be set to CH1 or CH2 and the input signal applied to the appropriate input connector. CH1 only displayed in STORE mode.

3.4.2 DUAL CHANNEL

For dual trace simultaneous display of both Y inputs against the timebase, this switch should be set to DUAL.

In the NORMal operating mode, two modes of beam switching are used and are selected automatically by the sweep rate selected by the TIME/CM switch. The alternate mode is used at fast sweep rates between 0.2ms/cm and 0.5μs/cm. At the slower rates from 0.2s/cm to 0.5ms/cm the chop mode operates at approx. 500kHz.

In the storage mode, CH1 only is displayed.

3.4.3 ADD

In the ADD mode, which is only available in the NORMAL operating mode, the single trace generated against the timebase is the algebraic sum of the CH1 and CH2 deflections.

If the INV CH2 button is operated the direction of the Y deflection for that channel is reversed. If used in the ADD mode, this facility allows the difference between the CH1 and CH2 inputs to be displayed. The INV CH2 button has no effect on the polarity of internal CH2 trigger.

When examining small differences between large signals, the effect of small errors between the sensitivities of the two channels can be overcome by first connecting one input to both channels simultaneously and adjusting one or other of the VARiable SENSitivity controls to obtain a straight line.

In the STORE mode, the ADD position of the MODE switch is equivalent to the CH1 position.

3.4.4 X–Y

In the X-Y mode, which is only available in NORMAL operating mode, the timebase is disabled and the CH2 input is displayed as the vertical Y deflection against the CH1 input displayed as horizontal X deflection. The CH1 shift control is inoperative and X position is determined only by the X shift control. The X10 MAG facility is also inoperative. X deflection sensitivity being determined by the CH1 controls only. The X bandwidth is limited to 1MHz and relative phase shift between X and Y delections may exceed 3° above 50kHz.

In the STORE mode selection of X-Y is equivalent to the selection of CH1.

3.5 TIMEBASE AND X-EXPANSION

The calibrated sweep speed of the internal timebase is determined by the setting of the TIME/CM switch and additionally in STORE mode by the ms–s button. When this button is in, the milliseconds section of the TIME/CM switch is converted to seconds, for example 1ms/cm becomes 1s/cm. In NORMAL operation the sweep rate may be varied by the VARiable SWEEP control, enabling intermediate sweep rates between the calibrated ranges to be obtained.

For horizontal shift of the trace, adjust the X shift control (horizontal arrows). If close examination of any portion of the trace is required, X10 expansion can be introduced by operation of the MAG Button. This provides an effective trace length of 100cm and any portion of this may be selected for viewing on the screen by operation of the X shift control.

3.6 TRIGGER

The timebase may be triggered internally from the CH1 or CH2 signals by operation of the corresponding

TRIGGER button, irrespective of whether the selected channel is being displayed. Alternatively, the timebase may be triggered from an external signal applied to the EXT TRIG sockets when both CH1 and CH2 buttons are operated simultaneously.

The + – button selects the slope, positive or negative going, which causes triggering when the signal passes through the level set by the TRIGGER LEVEL control. Presence of a TRIGGER signal is indicated by the associated TRIGGER l.e.d. This will flash at low trigger repetition rates and remain on at faster rates. Normally triggering can be obtained from internal deflection signals greater than 2mm pk/pk up to about 2MHz but the sensitivity reduces to about 1cm pk/pk at 20MHz. Corresponding external sensitivity is 0.25V pk/pk to 2MHz and 1.25V pk/pk at 20MHz.

With AC coupling, the low frequency sensitivity reduces to 1cm pk/pk at about 2Hz.

The Ext Trig input impedance is approx. 100kΩ/10pF and care should be taken not to apply more than 250V d.c. or pk, a.c. to this socket.

When the BRIGHT LINE ('BR LINE') button is out or ON, the timebase will free run in the absence of a correct trigger signal, to display a bright line or unsynchronised display until the level control is adjusted and/or the amplitude of the trigger signal is increased. This free-run action in the absence of correct trigger, helps in finding the trace and leads to ease of operation. If the timebase is required to free-run continuously, the LEVEL control should be set to either end of its rotation.

It is expected that the BRIGHT LINE OFF mode will be selected only when the instrument is to be used to display signals at repetition rates less than 40Hz or faster than 2MHz. This will prevent additional free-run sweeps from occuring between correctly triggered low frequency sweeps or erratic high frequency operation.

The coupling of the trigger signal may be selected as a.c. or d.c. by operation of the corresponding TRIGGER button. When both are pressed, an active synch. separator circuit is introduced to provide line or frame triggering for video waveforms. Field trigger occurs at low sweep rates up to 100μs/cm and line trigger is automatically selected at fast sweep rates from 50μs/cm. The trigger polarity should be selected for the polarity of the synch. pluses. At least 2mm pk/pk of synch. pulse amplitude is required with internal triggering, or 0.25V with external.

Summarising the use of the trigger controls for most applications:

(a) With BRIGHT LINE ON (button out), select the trigger source CH1, CH2 or EXT and the coupling required, AC or DC.

(b) Select the trigger slope + or – and adjust the trigger level control to obtain a trace which is triggered at the required point.

3.7 STORE CONTROL

STORE mode is selected by depressing the NORM/STORE button. The various STORE modes are selected by operation of the buttons on the right hand side of the NORM/STORE control, and by the buttons on the right hand side of the TIME/CM switch. All controls associated with the STORE mode are labelled in blue.

3.7.1 NORM/STORE

With this button out, NORMal operation is obtained. The instrument behaves like a conventional 20MHz oscilloscope. All controls associated with STORE mode have no effect.

With the button in, STORE mode is selected and the display is produced by the reading out of a digital store. Acquisition of data for this store, and the subsequent display of this data is controlled by the controls labelled in blue.

3.7.2 ROLL/REFRESH

Selection of ROLL provides a form of free running timebase not found on a conventional oscilloscope. Incoming data is fed continuously to the store. As the display is thus updated, the trace appears to be moving or rolling to the left, in appearance, similar to the view through a 10cm window of a strip chart recorder trace.

As information is being continuously written into the store, at a trigger instant the store will only contain pretrigger information. Thus by using the single shot facility (see 3.7.3, 3.7.5) pre-trigger information even for transient signals may be stored and displayed.

The rate of rolling is controlled by the TIME/CM switch and ms–s button. At high roll speeds the display becomes meaningless to the user, so for the top three ranges of roll mode, 0.2ms/cm, 0.1ms/cm, 0.05ms/cm, the display is blanked while information is stored in the memory. Once the information has been acquired ready for display, the store is read out once, and then, if release mode has been selected, the store is again updated and the display again blanked; the cycle of acquisition then display repeating until an alternative mode is selected. If trigger signals are not present and BRIGHT LINE is off the display will be blank on these three ranges until a trigger signal is present. The display on these three ranges still has a pretrigger facility in the released roll mode. Roll mode can be used on ranges 50sec/cm up to 0.05ms/cm.

If REFRESH is selected, the display obtained is similar to that obtained on a conventional oscilloscope but with the advantage of flicker-free operation at low timebase speeds. The display updates from the left hand side of the screen on receipt of a trigger as in conventional operation. If the instrument is in single shot mode (see 3.7.5) or the trigger is not present the display retains indefinitely the information captured on the previous sweep until a trigger is received in released mode or the instrument is rearmed. On the top three ranges of the TIME/CM switch for which refresh is applicable

0.2ms/cm, 0.1ms/cm, 0.05ms/cm, the display is blanked while the store is filled and then read out once when the acquisition is complete; this cycle repeating if in released mode, or if in single shot mode readout is then continuous. As in roll mode the display will be blanked if a trigger signal is not present, unless the display has been held or stored. Refresh mode is only used on ranges of 50s/cm to 0.05ms/cm of the TIME/CM switch.

3.7.3 PRETRIGGER/25% + 75%

These two buttons select the amount of pretrigger required when using the Roll mode single shot facility (see 3.7.2 and 3.7.5). With both buttons out, 0% PRETRIGGER is selected, with only the 25% button depressed 25% PRETRIGGER is selected, similarly for the 75% button, and with both buttons depressed 100% PRETRIGGER is selected.

The amount of pretrigger selected determines the percentage of the display which is acquired before the trigger point, and hence the position of the trigger point on the display. For example, if a trace is stored with 25% Pretrigger selected, the trigger point is 2.5cm from the left hand side of the display, the first 2.5cm of the display is pretrigger information, and the last 7.5cm is posttrigger information.

Pretrigger as mentioned earlier is available in the roll single shot mode, but on the three top ranges of the TIME/CM switch for which roll is available, 0.2ms/cm, 0.1ms/cm and 0.05ms/cm, the pretrigger facility is available in the released roll mode also (see 3.7.2 and 3.7.4). On these ranges a 'refresh' type display is obtained but with the position of trigger point being selected by these buttons.

3.7.4 RELEASE

Operation of this button puts the instrument into its continuous acquisition mode. In ROLL this means that the display 'rolls' continuously and ignores triggers except on the ranges 0.2ms/cm 0.1ms/cm and 0.05ms/cm (see 3.7.2). In REFRESH the display updates until the display is filled with new information and then updating ceases until a trigger is received. The display will again begin updating from the left hand side of the screen. This cycle of refreshing the display, then awaiting a trigger, repeats indefinitely in the released refresh mode.

Release does not separate on timebase ranges of 20μs/cm to 0.5μs/cm.

3.7.5 ARM

This button when operated initiates the single shot storage facility of this instrument. On arming, in ROLL mode, the trace will roll across the screen, and the ARMED/STORED l.e.d. will begin flashing.

When a trigger is received the l.e.d. will cease flashing and switch off. Meanwhile the trace continues rolling, and and after the required amount of pretrigger information is obtained, the instrument will accept a trigger, and when the required amount of post trigger information has been acquired the trace will cease rolling and the ARMED/STORED l.e.d. comes on continuously. The display will not now alter unless rearmed, or put into release mode by operating the release button. In refresh, operation of the ARM button stops the display updating if currently occurring and initiates flashing of the ARMED/STORED l.e.d. On receipt of a trigger the display will begin updating from the left hand side of the screen and the l.e.d. will cease flashing. When the display has been fully refreshed the STORED l.e.d. will come on. This display will now not alter unless rearmed or released.

3.7.6 ms–s

When this button is out the TIME/CM milliseconds ranges remain correct. However, when the button is depressed this multiplies the TIME/CM millisecond ranges by one thousand converting the millisecond/cm ranges to second/cm. It has no effect on other timebase ranges.

3.7.7 DISPLAY HOLD

Operation of the DISPLAY HOLD freezes the display so that no further modification of the display can occur. It can be used in ROLL mode to freeze the display if a feature of interest appears on the screen. Alternatively it can lock the display in REFRESH mode. Once the trace is frozen it can be plotted using PLOT 1 or PLOT 2 as required.

When the button is released, the instrument returns to a RELEASE mode. Hence operating HOLD will clear and ARM condition.

It should be noted that movement of the function switches after a display has been locked can disturb the display, particularly shifting the start point of the trace.

3.8 ADDITIONAL FACILITIES

1. Calibrator.
   This output pin on the front panel provides a positive going 1V flat topped square wave at approx. 1kHz. It can be used to check the sensitivity of the instrument or to set to any particular calibrated sensitivity (see section 3.3.4). The rise time is approx. 2μs and the output impedance is approx. 470Ω, providing approx. 2.3mA when shorted to ground.

   The CAL output may be used also to set up passive probes (see section 3.7.4).

2. Z mod.
   This socket on the real panel allows modulation of the brightness. The input is d.c. coupled into approx. 10kΩ/10pF. The sensitivity at normal brightness setting requires about 2V to provide visible modulation. Approx. +40V is required to provide full trace blanking.

   Care should be taken not to apply more than

100V d.c. or pk, a.c. to this socket.

3. Use of the Passive Probe
A X10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input resistance of a Y channel is 10M ohms, shunted by approximately 28pF. The effective capacitance of the input lead must be added to this and the resultant impedance can often load the signal source. Therefore it is advisable to use a 1M ohms, X10 probe such as PB12 or PB13. This reduces the input capacitance and increases the input resistance, at the expense of a 10X reduction in sensitivity. The probe inserts a shunt RC network in series to form a 10:1 attenuator with the input RC of the Y channel. To obtain a flat frequency response it is necessary to adjust the capacitance of the probe to match the input capacitance of the Y channel as follows:
   1. Set the Y channel VOLTS/CM switch to 20mV, the TIME/CM switch to 500μs and trigger from the appropriate channel.
   2. Connect the probe to the CAL socket.
   3. Adjust the probe compensation to obtain a level trace, i.e. flat top without overshoot or undershoot.

4. Camera.
A camera may be used with the oscilloscope to record waveforms. Suitable camera utilising Polaroid film may be obtained from Shackman and hand held against the tube face. Other oscilloscope cameras may be used but suitable adaptors must be obtained and should be discussed with the camera manufacturer.

To aid component location, circuit references have been allocated in the following general pattern.

1	–	99	Components not mounted on printed circuit boards.
100	–	199	Components mounted on the attenuator assemblies.
200	–	299	Pre-amplifier and Ramp Generator components mounted on the daughter board.
300	–	399	Y Pre-amplifier and Beam Switch components mounted on the main board.
400	–	499	Y Amplifier and Y Output Amplifier components mounted on the main board.
500	–	599	Timebase and X Output Amplifier components mounted on the main board.
600	–	699	Trigger circuit components mounted on the main board.
700	–	799	Power Supply and Modulation Circuit components on the main board.
800	–	999	Digital Storage Board and associated components.
1100	–	1199	Function Switch Board and associated components.
1200	–	1299	Auxiliary Power Supply Board and associated components.
1300	–	1399	Pick off Board and associated components.
1400	–	1499	Plot switch Board and associated components.

4.1 GENERAL

With the NORMal/STORE button out the instrument behaves as a conventional oscilloscope. Referring to the block diagram (Fig. 1) signals applied to the CH1 and CH2 input sockets pass into their respective attenuators and amplifiers. The VOLTS/CM switch controls the gain of the pre-amplifier in steps 1.2.5 sequence to cover the ranges from 2mV/cm to 0.1V/cm and a ÷100 attenuator is introduced before the amplifier on the ranges 0.2V/cm to 10V/cm.

The Variable Gain control adjusts the amplifier gain to give 1 to 2.5 times reduction of gain on all settings of the Volts/cm switch. The fast electronic beam switch selects either CH1 or the CH2 signal to be applied further and passed to the Y deflection plates of the c.r.t.

A sample of each signal is taken and passed to the trigger switch bank where selection of CH1, CH2 or Ext trig source is made.

The selected signal is amplified and passed to the Schmitt trigger, the output of which clocks the timebase bistable "on". The ramp generator then begins to generate its linear ramp, which, after passing through the X amplifier, is applied to the X deflection plates of the c.r.t. and drives the electron beam linearly across the tube face. A portion of the signal from the ramp generator is fed back to the hold-off circuit, shutting the gate to prevent any further pulses from the Schmitt trigger from reaching the timebase bistable during the ramp period. When the ramp has reached the necessary maximum level, the timebase bistable is reset, and the ramp is quickly returned to its quiescent state. A time-constant in the hold-off circuit retains this signal to inhibit another ramp from being initiated for a short period, until the ramp timing capacitor is discharged fully. Thus a ramp is generated at a rate set by the TIME/CM switch when the trigger signal reaches a pre-determined level. This ramp sweeps the beam across the c.r.t. face, returns and waits for the next input cycle to reach the set trigger point, so producing subsequent ramps. The timebase bistable is connected to a blanking amplifier whose function is to turn on the electron beam during the sweep and blank it off during the fly-back and subsequent waiting period.

At fast sweep rates for a dual trace display, the TIME/CM switch automatically selects the alternate sweep mode of control for the beam switch. At the end of each sweep, the signal from the timebase reverses the state of the beam switch bistable, causing alternate displays of the CH1 and CH2 signal on successive sweeps of the timebase. At slow sweep rates, the chop mode is selected, when the chop multivibrator free runs independently, causing the beam to switch or chop between CH1 and CH2 levels during the sweep.

A signal from the multivibrator also blanks the trace during each switching transition. With CH1 or CH2 only selected, the beam switch bistable is held to select that channel only. In the X-Y mode, the bistable is held to select CH2 as the Y deflection signal, while an additional switch diverts the output from the CH1 pre-amplifier to the X output amplifier, as the X deflection signal in place of the normal ramp signal. The blanking amplifier is held in the bright-up state. When TV trigger mode is selected, an additional synch. separator circuit is introduced into the signal path leading into the trigger amplifier.

When the NORM/STORE button is in the instrument becomes a digital storage oscilloscope. The output of the Y dot joiner is routed through to the Y output amplifier. Analogue signals from the CH1 preamp are picked off, buffered, then fed into a sample and hold circuit. The output of the sample and hold is routed into the Analogue to Digital Converter (ADC). This produces an 8 bit binary code representing the amplitude of the instantaneous signal input at 500 nanosecond intervals. The data produced is loaded into the store under control of the timing logic. The store can hold 1024 8 bit words and the data is entered at such a rate that the information contained in the 1024 bytes of memory represent one complete sweep of channel 1.

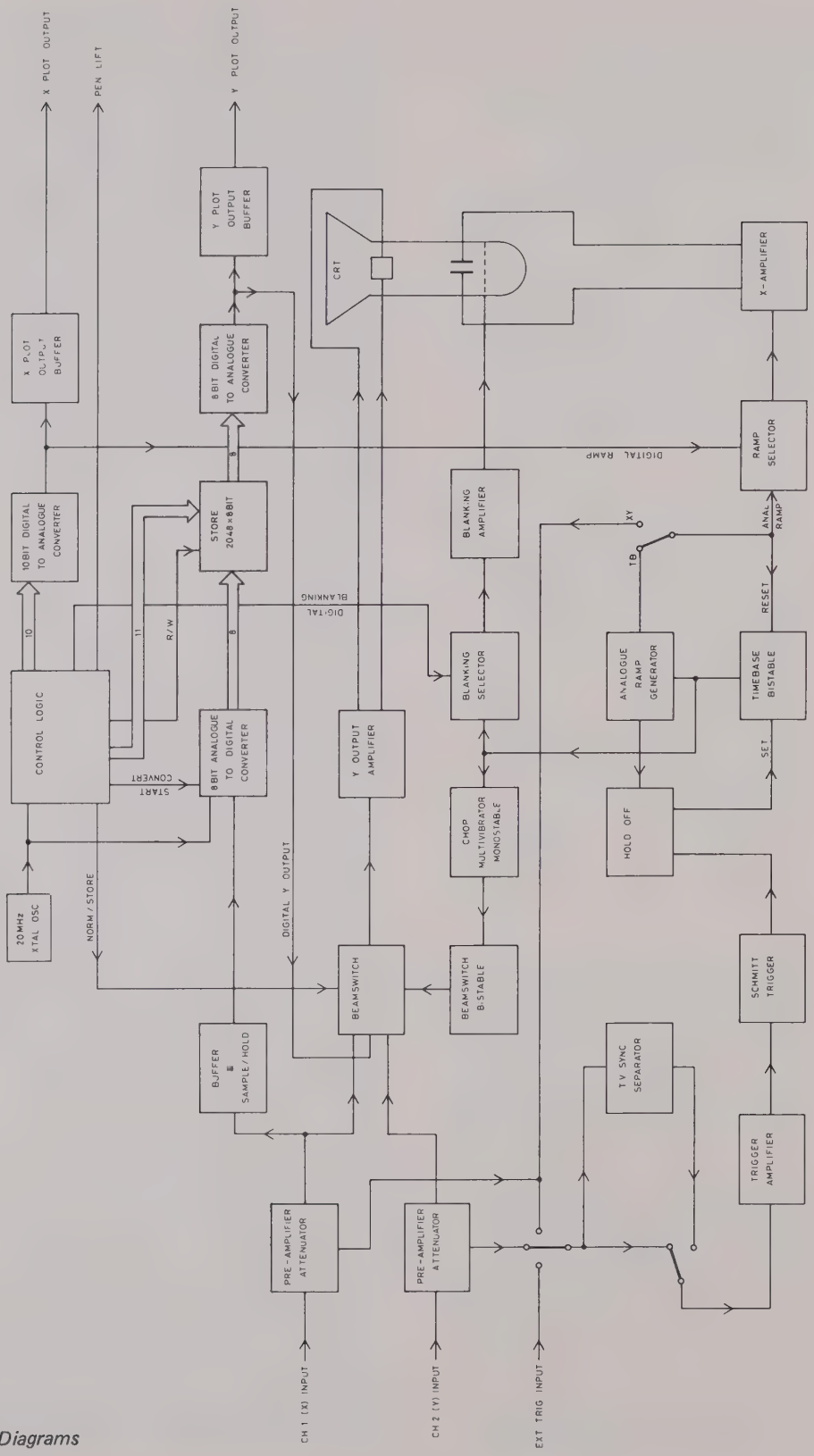


Fig. 1 Block Diagrams

This data is then read out (non destructively) at a fixed rate and reconstructed as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output to give a continuous display of the store contents. Since the output of the DAC is in the form of discrete levels a dot joiner is included to join these levels and provide a continuous display.

In all the digital storage modes the timebase sweep is controlled by a ten bit counter which provides an increasing ten bit code which is reconstructed by a ten bit DAC and dot joiner to give an analogue ramp. This ramp is synchronised to the readout of the Y data from the store. This ramp is used to display the 1024 bytes of store. The trigger is now entirely dissociated from the timebase since the latter runs continuously. The function of the trigger now is, in REFRESH to initiate a write cycle, during which a screen full of new information is entered into the store, and in ROLL when it is used to define the amount of pretrigger and post trigger information held in the store.

The trigger still produces an analogue ramp, but this is not used in STORE mode. In ROLL and REFRESH the rate a which data is entered into the store is defined by a programmable digital divider which divides the master 20MHz clock under control of the TIME/CM switch to provide 100 data samples per cm unexpanded on the display. This is also the resolution obtained in the SAMPLING mode. Expansion of this display is carried out in the X amplifier by analogue means and this gives a resolution of 10 samples/cm.

4.2 THE Y AMPLIFIERS AND BEAM SWITCH

These circuits are shown in Fig. 7, Fig. 10.

The attenuators and pre-amplifiers of channel 1 are identical to those of channel 2 and accordingly only channel 1 is described.

The input signal is applied to SKA and then to the attenuator via the 3 position slide switch, S101. This allows the input signal to be directly coupled through in the DC position or coupled via C105 in the AC position. In the central GND position, the input signal from SKA is left open circuited while the input to the attenuator is grounded.

On the most sensitive ranges, 2mV/cm to 100mV/cm, the VOLTS/CM switch, S102, couples the signal through directly to the pre-amplifier, and the network resistor, RN101c, provides the input impedance. On the remaining ranges, S102 introduces R101a into the signal path to form a 100:1 attenuator with RN101b in parallel with RN101c.

High frequency compensation of the attenuator is provided by C101 and C104, while C102 with C106 allows the input capacitance of the attenuator to be set to equalise that of the unattenuated ranges.

Diodes, D201 and D202, with R207 provide input protection by limiting the input voltage applied to the amplifier to the voltages of zener diode, D203 and the positive supply line.

The input stage of the pre-amplifier is formed by the f.e.t. source followers, TR201 and TR202, and emitter followers, TR204 and TR203. Unbalance in this stage is corrected by the BAL control potentiometer, R301.

The input stage drives the divider network, RN201. The VOLTS/CM switch second wafer, S201, selects the necessary output, either directly via RN201 on the 2mV or 200mV ranges, or attenuated by 2.5, 10, 25 or 50 times on the subsequent ranges. This network presents a constant output impedance and further attenuation is introduced by the shunt action of the VARIABLE sensitivity control, R217. The resultant signal is amplified by the integrated amplifier, IC301. The amplifier gain is determined by R309 and the preset, R302. The differential output is balanced by the bias through R308 from the preset, R307.

The differential outputs from IC301 are then split. A high impedance amplifier buffers the signal to the Analogue to Digital Converter (ADC) and converts the differential signal to a single ended output. (See Analogue to Digital Converter). The differential outputs also feed R316 and R317, which provide defined signal currents to the beamswitch, and these are summed with the Y shift currents defined by R318 and R319 from the CH1 shift control, R315. The corresponding components for channel 2 are R366, R367, R368, R369 and R365. Channel 2 only differs for channel one by the addition of the double pole changeover switch, S301, which reverses the output signals from IC351 in the INVERT mode. However, channel 2 is not picked off for the ADC.

The signals currents from IC301, and IC351 are fed into a 3 way beamswitch with the stored signal from the Digital to Analogue Converter (DAC). The beamswitch is formed by diodes, D301, D302, D303, D304, D351, D352, D353, D354, D811, D812, D813, D814. In NORMal mode the output of inverter U826e is low, switching off Q806 and Q807, it also takes the junctions of D811 and D813 low, diverting the signal currents from R823 and R824 reverse biasing D812, D814. The junctions of D301, D302 and D351, D352 are then both under control of IC501b. The bistable controls the beamswitching of the two Y channels into the Y output amplifier (see 4.5 Mode Control Circuits). In STORE mode the output of the inverter U826e is high. This forces the junctions of D301, D302 and D351, D352 low via Q806, Q807, diverting the Y preamplifier signal from the Y output amplifier.

At the same time, the junction of D811, D813 is taken high, forward biasing D812 and D814 and allowing the

signal from the Y DAC to drive the bases of TR401 and TR402 in the Y output amplifier. The outputs from the differential shunt feedback amplifier stage formed by TR401 and TR402, are fed to the ground emitter amplifier stage, TR403, and TR404. This in turn feeds the differential cascode Y output stage TR405, TR406, TR407 and TR408 to drive the Y deflection plates of the c.r.t.

High frequency compensation of the output amplifier is provided by networks between the emitters of TR403 and TR404 and those of TR405 and TR406. Adjustment of this compensation is by C402 and C405.

4.3 TRIGGER CIRCUITS

These circuits are shown in Figs. 8 and 10.

The Trigger Source switches, S502 and S503, connect the required trigger signal via the Trigger Coupling switches, S504 and S505, to the trigger buffer amplifier formed by TR601 and TR602. S502 selects the differential CH1 signal via R313 and R314 from IC301 (Fig. 4). S503 selects the equivalent CH2 signal via R363 and R364 from IC351. Where both S502 and S503 are selected, both of the above signals are disconnected and the single-sided input from the EXT TRIG input socket SKC is selected.

When the AC coupling switch, S504, is out, the trigger signals are directly coupled-through, but when this switch is in, AC coupling is introduced via C603 and C604 (C601 on External). TR601 and TR602 form a differential buffer amplifier with the DC balance controlled by the TRIGGER LEVEL control, R602. The differential output from this stage is applied to the comparator, IC602, which has positive feedback applied by R623 to form a Schmitt trigger circuit. The change-over switch, S506, reverses the output from TR601 and TR602 to determine the trigger slope.

When both S504 and S505 are "in" (AC and DC in for TV mode), the junction of R603 and C610 is connected to the −11V supply, D601 and D608 are brought into conduction while D602 and D604 are reverse biased. This diverts the output of the trigger amplifier away from IC602, into TR605, which amplifies the positive tips of the video waveform only. TR605 is prevented from saturation by feeding back the peak detected synch. pulses via TR607 and TR606 to the emitter of TR605. These pulses are amplified by IC601b and applied via R617 and D603 to the Schmitt trigger, IC602. IC601a is used in conjunction with S504 and S505 to disable the synch. separator when AC or DC is selected.

At the fast timebase sweep speeds, S262a is open and TR603 is cut off. However, at speeds of 100μs/cm and slower, R608 is connected to +11V and TR603 is switched on. This effectively grounds C609 to introduce an RC integrating time constant into the synch. pulse signal time path in the TV mode to separate out frame trigger.

The output of IC602 is used by the timebase generator (see next section).

4.4 ANALOGUE TIMEBASE GENERATOR AND X AMPLIFIER

The square wave trigger output from IC602 is applied (with d.c. bias of zener diode, D605) as the clock to the D type TTL flip-flop, IC501a. A positive-going trigger edge will clock the bistable driving $\overline{Q}$ low. In the waiting state. $\overline{Q}$ was high (+4.5V), turning on TR261 via R507 and R262, holding the input, and hence the output of the operational amplifier, IC261 at 0V. This timebase amplifier is connected as a direct voltage follower.

When the trigger signal sends $\overline{Q}$ of IC501a low, the timebase clamp transistor, TR261, is turned off. Part of the constant current generated by TR264 flows through the resistor network, RN272, to charge C263 at a constant rate. The resultant positive-going linear ramp voltage generated at the input of IC261 is buffered by that amplifier to generate the low impedance ramp output.

The timebase range switch, S262, selects the tap point on the network, RN272, to vary the ramp slope in the 1.2.5 sequence over a range of three decades. On all fast sweep ranges, TR262 is biased-off but on ramps 0.5ms/cm and slower, S262c connects R263 to +11V. TR262 is turned on and C264 is effectively connected in parallel with C263 to slow the sweep rate 1000 times.

The constant current into the ramp generator is derived from the current mirror circuit formed by TR262 and TR264. The variable gain control, R261, provides an approximate 3:1 range of variation in this current, R506 provides a preset calibration control on the slow sweep rates, only when S262c is closed.

When the ramp reaches its maximum level the negative bias, introduced by R521 and R519, is overcome and TR503 turns on, driving the reset input of the timebase bistable low. As the bistable switches, $\overline{Q}$ returns high and TR261 conducts to discharge the timing capacitor(s) and the sweep is complete. However, a hold-off action takes place to inhibit trigger signals during sweep and this remains for a short period after a sweep to ensure that the ramp potential is fully reset before the next sweep can be triggered. As the ramp goes positive, D506 conducts to charge C502, reverse biasing D503 and turning on TR502. At the end of the sweep when the timebase bistable is reset, $\overline{Q}$ goes low and the D input follows via the action of D508 and R511. The ramp output returns rapidly towards 0V but TR502 remains in conduction for a period determined by C502 and R518. Only when TR502 turns off can R516 and D507 take the D input high for the bistable to respond to the next clock input.

TR501 acts in a way similar to TR262 (described above) to introduce additional hold-off time through C501 on the slower half of the timebase ranges.

The bright line facility causes the timebase to free-run in the absence of trigger signals. The square wave output from the Schmitt trigger, IC602, is coupled via C615 into the peak detector diodes, D606 and D607, to generate a positive-going signal into the –ve input of IC601c driving its output negative. In the absence of such trigger signals for a period determined by C618 with R627 and R626, the output of IC601c goes positive. When TR502 turns off at the end of the hold-off period, D509 conducts to turn on TR504, driving the set input low to initiate another sweep.

This free-run condition is removed as soon as IC601c detects an output from the Schmitt trigger. When the o/p of IC601c is low it indicates the presence of a trigger signal. Q815 is then switched on, lighting Trigger l.e.d. D1.

This free run condition can be inhibited by operation of the BRIGHT LINE OFF switch S501 which takes the junctions of D509 and D505 low via R562.

The output of the ramp generator IC251 is fed to the analogue multiplexer U821b. The other input of the multiplexer comes from the output of the sample and hold U830 in the digital ramp generator (see digital ramp generator). In NORMal mode the ramp output from IC261 is selected by the output of U826e going low. The ramp is then buffered by U827, a unity gain buffer amplifier, and drives the X output amplifier via R821 and C820. In STORE mode, the output of the digital ramp generator is selected and as in NORMal mode drives the X output amplifier via amplifier U827, R539, and C515.

The X output amplifier is formed by the shunt feedback stage of TR509/TR511 driving single sided into the amplifier stage, TR513 and TR514. The collector output of this stage drives the X deflection plates of the c.r.t. directly from TR514 and via emitter follower TR515 and TR513. The gain introduced by TR509/TR511 is defined in the X10 magnification mode by the input resistance, R539, and the feedback resistance, R552, with the preset, R553. In this mode the transistor switch, TR512, is biased off. However, in the normal X1 magnification mode S507 is open and the current in R548 turns on TR512, introducing R544 with preset, R511, as additional feedback to reduce the gain of the amplifier accordingly.

The X shift control, R271, introduces an additional bias input via R541 and emitter follower TR506, through the potential divider R569/R545.

4.5 MODE CONTROL CIRCUITS

The display mode is controlled by S261 (fig.8) and the NORM/STORE button S.

S261 defines the state of three control lines L1, L2, L3. The state of these control lines is then further defined by the gating U822a, f, d, e, U823a, b, c, d U832a, b, c, U833a, d. The outputs of this gating DL1, DL2, DL3 are level shifted by Q808, Q809, Q810, and these outputs drive the mode control circuitry.

In NORMal mode, the state of DL1, DL2, DL3 follow L1, L2, L3 but in STORE mode these outputs do not follow L1, L2, and L3 (see table below).

NORMAL MODE

DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	IC501b Q	IC501b 5
X-Y	+11V	0	+11V	+11V	0	+11V	L	H
CH1	0	+11V	0	0	+11V	0	H	L
DUAL	+11V	+11V	0	+11V	+11V	0	SWITCHING	
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	0	0	0	H	H

STORE MODE

DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	IC501b Q	IC501b Q
X-Y	11V	0	+11V	+11V	0	0	L	H
CH1	0	+11V	0	+11V	0	0	L	H
DUAL	+11V	+11V	0	+11V	0	0	L	H
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	+11V	0	0	L	H

Section 4.2 described the action of beamswitching diodes, D301 to D304, D351 to D354 and D811 to D814, and as mentioned then in NORMal mode the diodes D301, D302 and D351, D352 are controlled by the outputs of beam switch bistable, IC501b. In the CH1 mode, DL1 is low allowing R525 to take the set input of the bistable low, Q is high and $\overline{Q}$ is low, selecting the channel 1 signal for Y display. In the CH2 and X-Y modes. DL1 is at +11V and R514 takes the set input high but L2 is open and R524 takes the reset input low to reverse the bistable and select the channel 2 signal.

In the Add mode, both DL1 and DL2 are low so that both set and reset are applied to the bistable, Q and $\overline{Q}$ are high and both channel signals are added into the shunt feedback stage of the Y amplifier (Fig. 4). In this mode only, DL1, DL2, and DL3 are open, removing the bias through D401, D402 or D403 and defined by R401 and R402 via D405 and D406. This offsets the additional bias introduced by the selection of both channel signals.

Only in the X-Y mode, DL3 is held at +11V to turn on the diode gate of D515 and D514, so coupling the channel 1 preamplifier signal of IC301, via TR506 and R547 into the X output amplifier. At the same time D504 conducts to turn off the gain switching transistor, TR512 thereby selecting x10 X magnification irrespective of the positive of S507.

D501 conducts allowing current through R509 to turn on TR261, clamping the ramp generator so that no signal is fed into the X amplifier via R539. Finally, current through R512 turns on TR504, holding the timebase bistable set "on" to provide continuous bright-up of the trace.

In the Dual mode, both DL1 and DL2 and held at +11V so that the beam switch bistable, IC501b, is free of set or reset signals. Thus it can respond to clock signals and as its D input is connected to its Q output its state reverses on each clock input.

On the fast sweep ranges (0.2ms/cm and above), the clock input is derived via emitter follower, TR505, directly from the Q output of the timebase bistable. Thus the beam switch operates in the alternate mode. The Y deflection is switched between channels at the end of each sweep. TR507 and TR508 form a free-running emitter coupled multivibrator but on the above ranges, S262 f is open such that R534 is disconnected and the multivibrator is disabled.

On the slow ranges (0.5ms/cm and below), R534 is connected to +11V and the multivibrator runs. During each sweep period, the multivibrator provides continuous clock inputs to the beam switch bistable so that the beam deflection signal is made to chop between the two channel signals. The beam switching is inhibited between sweeps as the emitter follower, TR505, clamps high the clock input to the beam switch bistable. In all modes but Dual, DL1 or DL2 are low and D512 or D513 conducts to inhibit the action of the multivibrator.

Ic601d is used for the 1kHz calibrator. It is connected as an oscillator with positive feedback via R629 and negative feedback via R633. This with C617 defines the frequency as approx. 1kHz. The output is buffered by the transistor switch, TR604, which defines the calibrator output amplitude via the potential divider of R638 and R643 with preset, R641.

In the STORE mode DL1, DL2, DL3, as shown in the table above, force all selections on S261 to be effectively CH2. The beamswitch bistable, IC501b then behaves as described above for this mode. However, since both outputs from the Y preamplifiers are disabled the beamswitch bistable does not control the input to the Y amplifier, and the Y amplifier is driven by the Y DAC.

4.6 THE ANALOGUE TO DIGITAL CONVERTER

These circuits are shown in Fig. 9, 10.

As described in Section 4.2 the differential CH1 Y Preamplifier output is picked off and converted into a single output on the pick-off board.

The CH1 outputs of IC301 are fed into a differential amplifier formed by Q1301, Q1302, whose gain is adjusted by R1329.

A sample of the shift amount set by R315 is also differentially amplified by U1301a. The gain of this stage is adjusted by R1323 and the offset by R1325, adjustment of these two presets enables matching of the shift signals and the Y signals. The output of U1301a is added into the output of the differential amplifier Q1301 and Q1302. The resultant signal is buffered by emitter follower Q1304.

The output of the emitter follower, Q1304 drives a sample-and-hold.

The output Q1304 feeds the sample gate formed by D801, D802, D803 and D804. Normally the diodes, D803, D804 are held reverse biased by the zener diodes, D803 and D804. The control circuitry produces a 50ns sample pulse, when a conversion is required at the output of U803c. This pulse is amplified and converted into a differential signal by a long tail pairs, Q803 and Q804. The differential output of Q803, Q804 is applied to T801 pulsing the Shottky diodes D804 and D803 on for the duration of the sample pulse. These diodes conduct and allow C803 to follow the analogue input from Q1304. When the sampling pulse ends the capacitor holds the instantaneous value of the input. The diodes have a very low leakage and the hold capacitor C803 is buffered by a very high impedance amplifier formed by Q801a, b and Q802. The capacitor therefore has a low droop rate and the output of the amplifier will be held for long enough for the successive approximation converter (SAC) to convert the analogue signal accurately into a digital representation.

The sample-and-hold holds the value of analogue signal at the sampling instant and its output is routed via Q803 to the SAC U815. The SAC has a 20MHz Xtal oscillator to control its internal logic. This is formed by U801f, U801e, C847, R867, R868 and XL801. The output of this oscillator is gated by U805b, so that the clock can be disabled externally and by the NORM/ STORE button, thus reducing the amount of break-through in NORMal mode. If the 20MHz clock is disable and external clock can be used via U802a.

The SAC conversion cycle is initiated as stated above by Start Convert. The conversion takes 9 20MHz clock cycles, i.e. 450ns, and it takes approximately 50ns for Start Convert to initiate the conversion. The complete conversion cycle takes 500ns. At the end of the conversion cycle the digital word representing the analogue input is latched onto the D0-D7 outputs. The SAC will nominally produce a code of 00000000 for an analogue input of 0Vand 11111111 for -0.5V the reference level input. However to compensate for the variation in gain of the pick-off buffer amplifier and sample-and-hold, the reference input to the SAC can be adjusted by R842 to −0.5V ±0.1V. This ensures that a CH1 input signal that causes a full screen deflection produces a range of codes from the ADC of 00000000 to 11111111.

4.7 TIMING AND CONTROL LOGIC

The timing signals used by the SAC are produced by the relatively high speed logic circuits around U807, a four bit decade counter. This counter is clocked by the 20MHz clock. Outputs QA QB, and QC which is inverted by U829d feed gate U805c which resets the bistable U806b on a count of three. This reset takes the Q output high. When the count reaches eight, QD goes high, clocking the bistable U806b, taking $\overline{Q}$ output low. Thus the WE input to U831 is high from a count of three to eight, which is a period of time of 250ns.

A counter output of eight is detected by U804a, the output of which goes low. On the next ninth clock this low is clocked through bistable U806a producing a positive going edge on the Q output. On the tenth clock the Q output remains low. This output therefore is a 50ns pulse that occurs on a count of nine of the counter U807. This pulse passes through two inverting gates U802c, U803b and is further delayed by U801a and U801b. This pulse clocks bistable U835d and also initiates a conversion cycle of the S.A.C.

The 50nS pulse at a 2MHz repetition rate, produced by U804a, is inverted by U809d and applied to U831 pin 54.

The LD input on Pin 9 of U807 is driven by U804c. One input of this gate will high when RESET STORED and/ or STORED (PIN 3 U831) are low. The other input of this gate will be high when RESCH1 (Pin 51 U831) is high. RESCH1 is driven high by U835b which is clocked by EWRITE (Pin 50 U831). The reset input of this bistable is controlled by the TIME/CM SWITCH.

A four bit code, D1, D2, DIV2, DIV5 is derived from this switch, from a double wafer on the pick-off board (See Fig. 9). The outputs are as shown in the table below:

TIMEBASE SPEED SELECTED	TIMEBASE CODE DIV2	DIV5	D1	D2
50ms/cm	1	0	0	0
20	0	1	0	0
10	0	0	1	0
5	1	0	1	0
2	0	1	1	0
1	0	0	0	1
0.5	1	0	0	1
0.2	0	1	0	1
0.1	0	0	1	1
0.05	1	0	1	1
20μs/cm	1	1	1	1
10	1	1	1	1
5	1	1	1	1
2	1	1	1	1
1	1	1	1	1
0.5	1	1	1	1

The output of gate U805a is high for all but the top six ranges when an all ones code is detected. This output is inverted by U826c. The output of this inverter is the SAMPLE signal. When SAMPLE is low, this takes the output of U809b high and hence the reset input of U835b low forcing RESCH1 high.

SAMPLE controls the selector formed by U802d, U802b and U803c. When SAMPLE is low, the Q output of U806a is routed through to the SAMPLE AND HOLD. via U802c and U803b. U806a hence controls the sampling of the input signals, the sample pulse being the same width and timing on the clock to the beamswitch bistable U835a described earlier in this section.

The waveforms described above are shown in Fig. 4.

4.8 STORE CONTROL

The data from the ADC is stored in a 1024 x 8 static random access memory. The timing signals controlling the writing of data into this store are produced by U831, an uncommitted logic array (U.L.A.). This U.L.A. produces a Read/Write control signal $\overline{NMWE}$ (see Fig. 5 for timing). This signal consists of 250ns pulses, at a rate determined by the TIME/CM switch. This signal latches the data from the ADC into a TRISTATE buffer U816 and controls the Output Enable line of this buffer. When $\overline{NMWE}$ goes low the data held in this latch appear on the outputs Qo to Qz. Simultaneously the output buffers of the memory are put into a high impedance state by this signal eliminating contention on the data bus. Meanwhile

U831 has produced a write address on lines A0 to A9 (U831 PINS 39,38, 37, 36, 35, 34, 32, 31, 30, 29). For each of the negative going pulses of NMWE A10 (U831 PIN 28) is low and when NMWE goes high again the data held in the buffer is stored in the address selected by A0–A9 and A10. When NMWE goes again, the new data from the ADC is latched into the buffer and again the stores' data lines go to high impedance. The lines A0–A9 contain a new write address so the new data is stored into next store location. When NMWE remains high in this way CH1 data is stored at a rate selected by the NMWE signal.

When NMWE goes high, the memory buffers are enabled and the stores will contain data from the address selected by A0–A10. Within the U.L.A. data lines, the write address is incremented after the write, reading of this data is again controlled by the U.L.A. U831. On all ranges below 0.2ms/cm reads are interleaved with writes at a 200kHz rate. Thus the address lines A0–A9 contain alternatively a write 'slot' and a read 'slot', each 'slot' lasting 2.5μs, enabling continuous reading and writing to occur. For all ranges above 0.5ms/cm, the store is completely filled with new data, then writing is prevented and store is read out. This process repeats, so that a complete write followed by a complete read occurs continuously, unless in a single shot mode when reads continue indefinitely after a complete write cycle.

The read and writes are interleaved continuously at 200kHz. rate so that for each new read 'slot' there is a new read address. This address is presented to the store which then places on its data lines the data contained at this address. At the end of the read slot RWCLK goes low, latching the Read Data into latch U819. The output of this latch drives the DIGITAL TO ANNALOGUE CONVERTER (see section 4.9). Note that in Roll mode, for ranges of the TIME/CM below 0.2ms/cm the read address will increment by two if a write has occurred in the previous write slot. This causes the continuous 'rolling' effect visible on the display in this mode.

The waveforms associated with the store control circuitry described above are shown in Fig. 5.

Once a 'read' of the lower 1024 addresses of the store is complete, A10 goes high for the next 1024 'read' slots so that the upper half of the store is read.

The process of converting and storing data has been described above. However, the selection of when a write cycle should occur and the associated operating mode are controlled by ARM RELEASE, 25% and 75% PRETRIGGER, ROLL/REFRESH and DISPLAY HOLD. ARM AND RELEASE control and when the data is captured in a single shot mode or in a continuous mode. The ARM button S1101 initiates a single shot acquisition of data. S1101 when operated, takes low the reset input of bistable, U814C, producing a low on the output R892 and R893 introducing hysteresis onto the reset input. The bistable output is inverted by U826d, and the resultant high level triggers one half of dual monostable, U1101, via input 2B, and allows timer, U1102, to oscillate at a period of 2Hz, set by R1107, R1106, R1108 and C1104, causing l.e.d. D1101, to flash at this rate. The time constant of this half of dual monostable, U1101, is set by C1102 and R1105 to be 100μs, and so on triggering, the Q output of this monostable will go low for 100μs. This negative going 100μs pulse arms the ULA U831. If the STORED output of this device was high, it will now go low. If REFRESH is selected by pushing in the ROLL/REFRESH button, the address lines of the U.L.A., during the write slots as described earlier in this section, remain at zero, until a trigger occurs. TRIGGER signals are disabled initially on ARM by latch, U835a. The latch is held set by S1101 and the $\overline{Q}$ output is low, disabling U812a and preventing triggers passing through this gate. When S1101 is released, the set input of U838a goes high after the length of the time constant set by C854 and R872. When the TRIG input next goes low it resets U838a taking the $\overline{Q}$ output high, enabling gate U812a and allowing triggers to reach U813a. When not in SAMPLING mode, the output of U805a is high, taking PIN1 of U813a high and PIN 11 low. The output of U812a will then be inverted by U813a, and triggers the U.L.A. when the TRIG input goes high. The output of U813a also drives U812b. The other input of this gate is high, again since $\overline{\text{RELEASE}}$ is high, taking low the output of U826f and forcing the output of U812c high. The inverted TRIG signal will thus take low the SET input of bistable U814c, forcing high the Q output, and low the output of U826d. This will take high the RESET on timer U1102 resetting the output, and switching off Q1101. The l.e.d. D1101 will extinguish.

Once the U.L.A. has received a trigger signal, the write addresses will increment from zero, at a rate determined by the TIME/CM switch, and at each successive store location, data from the ADC will be stored, as described earlier. When all 1024 store locations have been updated, the stored output of U831 will go high, taking low the output of U8046, high the output of U809a, and low the output of U829e. The STORED LED D1101 on the functions switch board will now light indicated that acquisition of data has now ceased and the display is now stored.

The operation of ARM in the ROLL mode is essentially as described above except that the write addresses begin incrementing immediately after the ARM to U831, and the ULA U831 ignores TRIG signals. When a sufficient amount of data has been entered into the store to satisfy the pretrigger requirements, the U.L.A. will now accept a TRIG signal. When the required amount of post trigger information has been stored, writing will cease and the STORED output of the U.L.A. will go high, as in REFRESH. As data is written into the store the read address increments so that an increasing offset occurs between the Read Address to the STORE and the address lines to the DAC, U818, causing a 'rolling' effect on the display. The display ceases

rolling when the STORED indication occurs, since writing ceases.

When ARM is operated, it also clocks bistable, U836a. The D input of this bistable is driven by gate, U824a. If the TIME/CM switch is selecting ranges 0.05ms/cm, 0.1ms/cm and0.2ms/cm, the output of either U833b or U833c will be low, taking high the output of U824a. If ROLL mode is selected the output of U824c will be low, again forcing high the output of U824a. The output of U824a therefore indicates that either one of the three timebase ranges mentioned above, or ROLL mode has been selected by S1105. Therefore the Q outputof bistable U836a will be low if ARM is operated and the output of U824a is high, forcing high the output of U824b, selecting ROLL mode to the U.L.A. until RELEASE or RESET or hold goes low, when the output of U824b will follow the state of the ROLL/REFRESH signal from S1105.

Operation of the RELEASE button triggers monostable, U1101, on the function switch board. The monostable has a time constant of 100μs set by R1104 and C1101. The monostable will thus produce a negative-going 100μs pulse which clears the STORED condition and resets U836a which enables the ROLL/REFRESH signal to the U.L.A. to follow the ROLL/REFRESH button. In refresh, the operation of RELEASE essentially enables continuous recycling of the write cycle described above for ARM. The write address holds at zero until a trigger occurs, at which point, the write address begins incrementing, data being stored in each successive location. When the STORE has been filled with new data, writing ceases until another trigger is received when the writing process begins again. This cycle repeats indefinitely until the operating mode is altered.

In ROLL after operation of the RELEASE button, the write addresses to the store begin incrementing immediately, new data being stored at each location in succession. Again as in the ARMed mode the read address to the store increments by one extra count after each write, causing the rolling effect on the display. The write process occurs continuously and is unaffected by the TRIGGER signal, and the display as a result will roll continuously, new data appearing on the right-hand end of the screen and rolling across the screen to the left-hand side.

On the top three ranges of the TIME/CM switch for which ROLL and REFRESH are applicable, 0.2ms/cm, 0.1ms/cm and 0.05ms/cm, the display is blanked while data is being acquired and then after acquisition is complete the new data is displayed. The rolling effect on both ARM and RELEASE is therefore not present on these ranges. However data is acquired in exactly the same fashion as described above.

The amount of pretrigger information stored in ROLL mode is controlled by the two button 25%, 75% PRETRIGGER. When both buttons, S1103 and S1104, are out the signals PER 25 and PER 75 are both low, and with either S1103 or S1104 operated the relevant signals PER 25 or PER 75 will go high to indicate 25% or 75% PRETRIGGER has been selected. With both switches operated both signals will go high indicating 100% PRETRIGGER selected. These two control signals PER 25 and PER 75 are used by the U.L.A. U831, to control the acquisition of data with respect to the trigger point. If REFRESH mode is selected control signals PER 25 and PER 75 will both be low, indicating 0% PRETRIGGER, regardless of the state of the two PRETRIGGER buttons, S1105 forcing a low output from both S1103 and S1104.

Operation of Display hold freezes the display, holding the information present on the screen. When the DISPLAY HOLD button, S1404 is out, the set input of bistable U814b is high, and the reset input is low. The Q output of U814b is therefore low, taking the output of U826b high. The D input of U836b is thus high and so when DACIO of U831 goes high, halfway through a read cycle the Q output will be clocked high, producing a low of the output of U824d, and taking N HOLD on U831 and one input of U809c high. The U.L.A. U831 will take a high level as indicating a NOT HOLD signal. The $\overline{\text{NMWE}}$ signals will reach the memory enabling data to be written to the STORE as described earlier.

If DISPLAY HOLD is operated, i.e. pushed in, the set input of U814b will go low and the reset input will now be high taking the $\overline{Q}$ output high. The D input of U836b will go low and when DAC 10 next goes high, during a read cycle the Q output will go low. This produces, a positive clock edge at U836a, latching either the state of the ROLL/REFRESH, or if the TIME/CM switch is on the ranges 0.2ms/cm, 0.1ms/cm and 0.05ms/cm, as described earlier. The N HOLD input of U831 is taken low, freezing the write address produced by the U.L.A. for the memory, preventing further locations in the store being updated. Gate U809c is also disabled driving high $\overline{\text{NMWE}}$, and hence preventing data being altered at the current write address.

4.9 DIGITAL TO ANALOGUE CONVERTER

The Y data present on the output of latch, U834, is converted into an analogue form by U820, a monolithic eight bit digital to analogue converter. A reference current is fed into this device and the Io and $\overline{\text{Io}}$ outputs produce a differential current output proportional to the product of this reference current and the digital code present on its data inputs Do to D7. Resistors, R886 and R887, set a reference current of 1mA, giving Io and $\overline{\text{Io}}$ a range of 0→ 1mA depending on the digital code selected. The reference current is derived from a 6V2 voltage reference formed by Zener Diode D821 and R885 decoupled by C859. Approximately one quarter of the Io and $\overline{\text{Io}}$ currents are fed into the differential amplifiers, U827a and U827d, which convert the currents into a voltage output of approx. +280mV.

A time constant of 1μs, set by C822 R830 and R831, is applied to this differential output. This matches the time

constant of the digital ramp generator, and provides a dot joining effect on the display, the dot moving linearly between the data points, though the brightness increases non-linearly as the dot moves between the data points. An adjustment of the relative d.c. offset of the differential Y output signals is provided by R829 enabling the two Y output signals to be balanced. The outputs of this amplifier is fed into Y beamswitch via R823, R824, R371, R372 as described in section 4.2.

4.10 DIGITAL RAMP GENERATOR

The U.L.A. provides a linearly incrementing address bus DAC1 to DAC10 to drive a 10 bit digital to analogue converter (DAC). The lines DAC1 to DAC10 increment from 0 to 1024 as the Y data is read out of the store, 0 corresponding to the left hand edge of the screen, and 1024 the right hand edge of the display. These ten signals are fed into U818, a monolithic 10 bit D.A.C. This produces the differential current outputs Io and $\overline{Io}$ which represents the product of the digital word on the data inputs and the reference current into the device. The reference current is set at 1mA by R845 and R846 which are connected to 0V(A) and the 6V2 voltage reference mentioned in the previous section.

The current $\overline{Io}$ which flows to U818 pin 2 derives from R844, the difference current feeding into R847. The voltage of 0 to +1V generated across R847 is buffered by the unity gain buffer, U825b (see Plot section 4.12).

The Io current output of U818 pin 4 is fed to amplifier, U825a, which converts it to a voltage output. The gain of this amplifier is set by preset, R834. A time constant of 1μs on the output is set by R833, R822 and C821 to match the time constant in the Y D.A.C. output amplifier (a small analogue ramp is added into the amplifier input in sampling if necessary. See 4.11) The output of the D.A.C. has a glitch at the changeover of the m.s.b. To reduce this a sample of the m.s.b. is fed into the inverting input of the output amplifier via R849 and C830. The output of the amplifier drives one input of the multiplexer U821b via R833. The other input of this multiplexer is the analogue ramp output from IC261. When NORMal is selected the analogue ramp is fed through to the X output amplifier, and in STORE mode the digital ramp is fed to the X output amplifier, U826e controlling the multiplexer.

The U.L.A. U831 produces a digital blanking signal which lasts for the first four counts of the count on lines DAC1 to DAC10, i.e. 20μs wide. This digital blanking signal is multiplexed with the analogue blanking signal from TR507 collector. In NORMal mode, the analogue blanking signal is selected and in STORE mode the digital blanking signal is selected, the selected signal driving the

Bright-up amplifier described in section 4.13, which provides blanking of the display when the c.r.t. beam flies back from the right hand side of the screen to the left hand side.

4.11 POWER SUPPLIES AND C.R.T. CIRCUITS

Circuits for the power supplies are shown in Figs. 10, 11. The following D.C. supples are generated in the power supply circuits from secondary windings on the supply transformer, T.l.

+ 210V, + 11V, + 12V, + 7V, + 5V, - 5V, - 11V - 1850V.

The + 210V line is used primarily in the X and Y output amplifiers. The -1850V line is the cathode supply for the c.r.t. An additional 5V line is generated in the timebase from the + 11V line by IC552 (Fig. 8).

The incoming a.c. supply from the supply connector, PLM, is switched by S1 and fuse protected by FS1 before reaching the two supply range switches, S2 and S3. S2 connects the two primary windings of T1 in series or in parallel for 120V or 240V operation while S3 selects the necessary tap for 100V or 220V operation.

The output from the 210V secondary is bridge rectified by the four bridge-connected diodes, D722 to D725, into the reservoir capacitor, C705. The resultant d.c. voltage protected by FS701 feeds the h.t. regulator for the +210V supply. D730 is the reference for this supply, buffered by emitter follower, TR711, and the Darlington pair, TR713. The return of the rectified 210V supply is via the 11V line to balance load currents in the low voltage supplies.

The four low supplies +11V, + 7V, - 5V (used on the main p.c.b. assembly), and - 11V are derived from a single 25V secondary of transformer, T1. Its output is bridge-rectified by bridge connected diodes, D726 to D729, into the reservoir capacitor, C704.

The distribution with respect to the 0V line of the voltage across this capacitor is determined by the -11V shunt regulator and the +11V series regulator. The -11V reference is provided by the sener diode, D711, with temperature compensation diodes, D713 and D714, and the shunt transistor, TR712, conducts to maintain the -11V line at the correct potential.

The -5V line is derived from this -11V line by the zener diode, D712, with the compensation diode, D720, followed by the emitter follower, TR709.

With the negative side of the unstabilised supply across C704 defined at -11V by that stabiliser, the positive side is applied to the series regulator, IC702, which takes up all variation in the unstabilised supply to define the +11V line. This is a 15V regulator with 'low' pin 3, returned to a -4V potential defined from the -5V supply by R735 and R734.

The +7V supply is provided from the +11V supply by a further 12V series regulator, IC701, operating with respect to the -5V line.

All the above outputs are connected to the subsequent oscilloscope circuitry via split pads in the copper track pattern. These are normally bridged by solder but can be used to isolate each line to assist fault finding.

The +12V, +5V and -5V supplies are derived from secondary windings on T1 of 14V, 8.5V and 8.5V respectively. The 14V output is bridge-rectified by D1205, D1206, D1207 and D1208 and smoothed by C1204 and C1205. A 12V regulator U1202 provides a regulated supply of 12V, which is decoupled by C1206. The +5V and -5V supplies are produced in a similar manner, the relevant components being D1201, D1202, D1203, D1204, C1201, C1202, U1201, C1203 and D1209, D1210, D1211, D1212, C1207, C1208, U1203 and C1209.

The grid and cathode supplies for the c.r.t. are derived via the voltage doubler circuit D718, D719, C711 and C712, from the 950V secondary of T1. The negative side of the unstabilised supply developed across C711 and C712 is held at approx. -200V with respect to 0V by the series zener diode, D706, which is returned to the stabilised cathode potential of -1850V. Subsequent variations in the unstabilised supply are developed across the series regulator, TR707, of the e.h.t. regulator. The feedback path of this regulator uses the current from the -1850V line defined by the resistors R715, R714 in parallel with R744 (the Focus pot.) and RN720e. The latter being within the e.h.t. network. This current is returned to the +7V line via R731, R725 and R726. If the resultant potential of the tap point defined by the preset, R725, is not at approx. -4.5V, the current in transistor, TR706 will change to correct the stabilising voltage across TR707, TR706 and TR707 are connected in cascode.

The heater of the c.r.t. is supplied directly from an independent 6.3V secondary winding of T1.

The OS1400 employs a novel modulation circuit to control the grid potential with respect to the cathode potential. The transistor pair, TR703 and TR704, generate an essentially constant current from the collector of TR703. This generates a constant voltage across RN720 and preset, R713, and is returned to ground via the output of the bright-up amplifier. Thus signal variations from this amplifier which operates with respect to 0V are transferred with the large negative d.c. offset to the collector of TR703, to be applied to the grid of the c.r.t. via the emitter follower, TR716.

In more detail, the constant current from TR703 is defined by the emitter resistance, RN720c and the base potential, from the divider, RN720a and RN720b.

This constant current source is returned to the -200V line (negative of D706) so that the collector of TR703 (the c.r.t. grid) can move negative from the cathode. The collector potential is protected by D705 against excessive swing during switch-on or switch-off conditions. While RN720d and R713 generate the necessary large d.c. potential to couple the bright-up signals to the grid, the high frequency components are by-passed through C702.

The bright-up signal amplifier is formed by the cascode transistor pair, TR701 and TR702, with shunt feedback via R704. It responds to the sum of three inputs. The first is a d.c. bias via R707 from the INTENSITY control, R745. The second is the external Z Modulation signal from SKG, via R703. The third is the signal from the blanking selector, U813a, which in NORMAL provides bright-up during each timebase sweep with blanking of each chop transition if appropriate, and in STORE mode provodes bright-up on each readout sweep. Diodes, D701 and D702, provide protection against excessive external inputs and with R702, prevent saturation of TR702.

The focus electrode of the c.r.t. is supplies from the focus control potentiometer, R744, with a portion of the -1850V supply. The astig. electrode is supplied from preset, R708 driven from the +210V supply via the divider network R746, R747.

Minor angular misalignment of the gun assembly of the c.r.t. or the effects of externally applied magnetic fields, axial to the c.r.t., can be corrected by the trace rotation coil. This coil is round the neck of the c.r.t. and the current is determined by the TRACE ROTATION control, R737, connected between the ±11V supplies and driving emitter followers, TR714 and TR715.

5.1 GENERAL

Fig. 2 and 3 show the internal location of the major components, subassemblies and preset controls. No regular maintenance is required apart from the routine recalibration. The construction of the instrument is such that full access to all calibration controls and to most components can be obtained once the two halves of the case have been removed (See section 5.2).

Supply voltage adjustment is made by the two selector switches on the rear panel. The supply fuse is mounted adjacent to these switches and the supply connector. This connector should be removed or the instrument switched off before operating the switches. For 100 or 120V operation a 500mA, 20mm slo-blo fuse is required (Part No. 33685), for 200 or 220V operation a 250mA, 20mm slo-blo fuse is required (Part No. 33684). The internal H.T. fuse is a 100mA, 20mm fuse (Part No. 32958).

5.2 REMOVAL OF THE CASE AND SUB-ASSEMBLIES

WARNING
DANGEROUS VOLTAGES ARE EXPOSED ONCE THE CASE IS REMOVED. MAINTENANCE SHOULD BE CARRIED OUT ONLY BY QUALIFIED PERSONNEL. PARTICULAR CARE SHOULD BE TAKEN ON THE C.R.T. AND THE E.H.T. AREA OF THE MAIN PRINTED BOARD WHERE VOLTAGES IN EXCESS OF 2000V ARE PRESENT. THESE VOLTAGES MAY BE RETAINED AS STORED CHARGE FOR UP TO ONE MINUTE AFTER THE SUPPLY IS DISCONNECTED.

(a) To remove the Cast (Top section)
DISCONNECT FROM THE SUPPLY.
Remove the two fixing screws at the top front sides and lift the top cover up and forward to clear the front moulded frame and the rear plastic moulded cover.

(b) To remove the Cast (Lower section) and Handle assembly.
DISCONNECT FROM THE SUPPLY.
Remove the two fixing screws at the top front sides and proceed to remove the top cover as detailed in (a) above. Rest the instrument upside down and remove the screw from the centre of the front frame, securing the cover. Lift the lower cover up and forward to clear the front moulded frame and the rear plastic cover. It may assist this operation if the screws holding the rear moulding are slackened but not removed.

(c) Removal of the C.R.T.
Remove the case as described in (a) and (b) above. Disconnect the trace rotation coil leads from pins 734 and 735 on the main printed circuit board. Unplug the tube base assembly. The base itself is carried on a small printed board which has been designed to allow access to facilitate withdrawal from the c.r.t. pins. Remove the single clamp fixing screw (see Fig. 2) and rotate the two clamp sections approx 30° to free the clip from the centre panel. Once the tube and clamp assembly are free the clamp itself can be slackened on the tube. Slide the tube backward through the centre panel until the c.r.t. face plate is clear of the front mounting clip. The tube can then be lifted up and drawn forward, to clear the top edge of the front panel and frame moulding of the instrument. Withdraw the tube from the shield and the two part clamp.

When fitting a new tube, operate in the reverse order to the above instructions, with the exception of the tube clamp and centre panel fixing screw. On re-assembly the fixed part (rear) of the c.r.t. clamp is located in the slotted locating holes in the bulkhead and the retaining screw is fitted. The tube is then held forward against the graticule in the front moulding whilst the clamping ring is rotated to hole and lock the tube in place. Do not over tighten this ring.

Check the polarity of re-connection of trace rotation coil leads. Clockwise rotation of the front panel preset control should cause a corresponding movement of the trace.

(d) Removal of the Attenuator assembly.

Should it be necessary during repair to remove the attenuator and screens around the pre-amplifier for access to components on that board or on the front of the main board, proceed as follows.

Remove the collet fitted knob on the timebase switch. Access to the collet securing screw or nut is by prising off the clip in the centre cap on the knob. Remove the small push on knobs on the two Variable Sensitivity controls, the Mode switch, the Trigger Level, the Variable Sweep and X Shift controls. Unsolder and, using a desoldering tool clear the solder from the three screens where they are earthed onto the pre-amplifier board.

Unsolder and remove the wires from the CAL 1V pin and the EXT trigger connection on the input printed circuit board. Unsolder also the two signal connections to pins 201 and 231 on the pre-amplifier board.

The sub section front panel, carrying with it the two attenuator volts/cm switches, the two AC/GND/DC switches and the input coupling printed board can now be un-latched by springing the four latch fingers away from the moulded frame and withdrawing the complete unit.

Re-assembly is the reverse of the aforementioned. Since the two attenuator switch wafers are symmetrical the shaft can be inserted in either of the two possible alignment positions.

(e) Removal of the Input Coupling Switch printed circuit assembly.

If it is necessary to gain access to the small printed board which carried the input selection switches and the A.C. coupling capacitors for each Y channel, together with the input network for the External trigger signal proceed as follows. Using a desoldering tool, unsolder the tags of the input screen, clear the holes of solder and remove the screen Unsolder and remove the two wires connecting the input printed board with the two attenuator wafer sections of each volts/cm switch. Desolder the three input B.N.C. sockets from this board and the three screen earthing points. The board should then be free for removal by easing upward, off the screen tags, then rotated to enable the switch sliders to clear the front moulding, and so withdrawn.

Re-assembly is the reverse of this sequence.

(f) Removal of the C.R.T. Control Potentiometer board.

If it is necessary to gain access to the control pots proceed as follows. Remove the push on knobs on the Focus and the Intensity controls. Ease the spacer retaining ears out of the printed board, so freeing the board from its retaining plastic spacer. Separate the two control pot shafts from the moulded shaft couplers. Full access to both the component side and the track side of the board is now facilitated and the faulty component can be readily accessed.

(g) Removal of the Pick-off Board

If access to the pick-off board for repair or maintenance is required, the D.S.O. p.c.b. can be easily removed. First remove all plugs and sockets from the D.S.O. board and then lift the board clear of the 3 supporting hinges taking care not to catch the trailing cable assemblies. This clears the area around the Pick-off Board, which is supported by two pillars on the edge near the c.r.t. and the switch wafer on the opposite side. Unscrew the nuts securing the wafer onto the switch shaft and slide the board off the two pillars and this shaft, taking care not to damage the wiring under this board. Remove the socket from the lower edge of the board and from the 16 pin DIL SKT next to the switch wafer on the reverse of this board. The board may now be lifted clear.

5.3 FAULT FINDING

Before any fault location is attempted, it is suggested that all supply voltages are checked. Subsequent signal voltages and waveforms should then be checked according to the following list, which may be used as a general guide and aid to servicing. Note that the typical voltages for unstabilised supplies are quoted for nominal mid-range supply voltages.

If a fault cannot be cleared it is recommended that the instrument is returned to the manufacturer for repair (see section 7).

When faults have been cleared it is recommended that the setting-up procedure of section 5.4 is followed.

For checking the supply lines there is a double row of test pins, separated by bridged split pads. These pins will give outputs of +11V, -11V, +210V, +7V and -5V and if required the currents drawn by each line can quickly be measured simply by breaking the solder shorting the split pad for normal working operation, and inserting a current measuring meter between the two pins. In all five cases the line feed is nearer to the rear of the instrument, whilst the line load is connected to the forward pin.

The +12V +5V, -5V supplies for the DSO board may be monitored on the D.S.O. board at PLPP pins 1 to 6.

Normal Operating Conditions
Unless otherwise specified the controls are set for single channel operation with the trace centred and timebase running. Potentials are specified with respect to ground and should be measured with a high impedance voltmeter, digital voltmeter or oscilloscope as appropriate. The NORMal switch should be set to NORMal unless otherwise specified.

(a) Supplies Unregulated

30V DC across C704 from 25 r.m.s. secondary voltage

268V DC across C705 from 210 r.m.s. secondary voltage

2.5kV DC across C711 + C712 from 950V r.m.s. secondary voltage

12V DC across C1201 from 8.5V r.m.s. secondary voltage

20V DC across C1204 from 14V r.m.s. secondary voltage

12V DC across C1207 from 8.5V r.m.s. secondary voltage

Stabilised

+210V	± 21V	
+11V	± 0.5V	
+7V	± 0.4V - 0.6V	
-5V	-10.4V, - 0.6V	
-11V	± 0.5V	
+12V	± 0.6V	From auxiliary supply board
+5V	± 0.25V	
-5V	±0.25V	

(b) Y-amplifier

Test Point	D.C. Level	Sensitivity
TR203/204 Collector	+7V	-
IC301, pin 1	+1V ±0.8V	-
IC301, pin 14	+1V ±0.8V	2mV/cm
IC301, pins 7, 8	+3.5V	65mV/cm each side

U827a	+3.9V	70mV/cm	With NORM /STORE
U827d	+3.9V	70mV/cm	switch in STORE

Test Point	D.C. Level	Sensitivity
TR401/402 Collector	+3.7V	40mV/cm each side
TR403/404 Collector	+7.7V	140mV/cm each side
TR405/406 Collector	+12.6V	-
TR4057/408 Base	+15.6V	-
TR407/408 Collector	+115V	6.8V/cm each side

(c) Analogue Ramp Generator

Test Point	Signal
Across R265 or R266	0.8V d.c. at "cal" 0.3V d.c. at min.
IC261 pin 3 and pin 6	+3.7V ramp from 0.1V level
TR264 Collector	+3.7V ramp from base level between 0 and +4V dependent on sweep rate selected.

(d) X-amplifier

Test Point	D.C. Level	Signal
TR512 Collector	+0.65V (Centre Screen)	500mV/cm 6.0V ramp
TR511 Emitter	+3.7V (Centre Screen)	500mV/cm 6.0V ramp
TR514 Base	-3.0V	-
TR513/513	+118V	12V/cm each side 140V ramp each side

(e) Trigger Amplifier

Test Point	D.C. Level	Signal
TR601/602 Base	0V on Ext. 0V on Int A.C.	65mV/cm each side
	+3.5V on Int D.C.	65mV/cm each side
TR601/602 Collector	-4.8V	25mV/cm each side

On TV mode:- TR601 and TR602 collector drops to between -8.5V and -10.5V dependent on the setting of the Trig. Level Control.

IC602, pin 9. Trigger output switches between -2V and -5.6V levels.

(f) Timebase Control

Test Point	Signal
IC501, pin 14	+5V, ±0.25V
IC501, pin 1	+5V (+1V at end of ramp)
IC501, pin 2	+4V (0v during hold-off)
IC501, pin 3	Trigger pulses between -0.5V and +2.8V levels
IC501, pin 4	+5V (0V during reset by bright-line)

Test Point	Signal
IC501, pin 5	+0.2V between sweeps +4.5V during sweeps
IC501, pin 6	+4.5V between sweeps +0.2V during sweeps
IC501, pins 8, 9	Beam switched between +0.2V and +4.3V levels
IC501, pins 10, 13	-0.6V or 4.5V depending on mode switch setting.
IC501, pin 11	Chop/alt. pulses between +0.2V and +4.7V levels
IC601, pin 8	+0.5V triggered or bright-line off +0V bright line operating
IC601, pin 9	0V triggered or bright-line off +9.5V bright line operating

(g) Bright-Up Amplifier

Test Point	Signal
TR507 Collector	Swtiching signal +4.8V (Blank) to 0V (Bright up)
U831 pin 52	Switching signal +5.0V to 0V (STORE selected on NORM/STORE switch)
TR702 Base	+2V
Collector	Between +6V and +48V dependent on intensity
RN720, pin 4	-2kV
RN720, pin 5	+50V with respect to pin 4
RN720, pin 6	+340V with respect to -1850V

(h) Analogue to Digital Converter

For following measurements set instrument into STORE mode at 0.5ms/cm.

Test Point	D.C. Level	Sensitivity
Q1302 Collector		65mV/cm
Q1304 Emitter	0V	65mV/cm
U1301a pin 1		65mV/cm
D804, D803 Junction	0V	65mV/cm
Q802 Emitter	-0.25V	65mV/cm
Q805, Q905 Base		
U815 Pin 16	-0.25V	65mV/cm
Pin 2	50ns pulse 0	4V signal
Pin 18	20MHz Clk.Switching 0	4V

(i) Control and Timing Logic

Instrument in STORE mode at 0.5ms/cm

Test Point	Signal (TTL Levels 1 = TTL high level 0 = TTL low level)
U807 pin 9	1
U804a pin 3	50ns Negative-going pulse
U805c pin 8	50ns Negative-going pulse
U806a pin 6	50ns Positive-going pulse
U801e pin 10	20MHz Clock
U802a pin 3	20MHz Clock
U8066 pin 8	2MHz Clock with even mark/space
U803c pin 8	50ns Positive-going pulse
U807 pin 11	100ns Positive-going pulse
U807 pin 7	1

(j) Store Control

Instrument in STORE mode at 0.5ms/cm

Test Point	Signal (TTL logic levels 1 = TTL high level 0 = TTL low level)
U831 pin 46	1
U831 pin 48	200kHz clock even mark/space
U831 pin 27	Two 250ns Negative-going pulses every 5μs
U831 pin 47	1 during ramp 0 during hold-off
U831 pin 52	20μs positive-going pulse every 5ms
U831 pin 18	5μs negative-going pulse every 5ms
U817 pin 21 U816 pin 1	Same as U831 pin 27
U816 pin 11	2 250ns positive-going pulse every 5μs

(k) Digital to Analogue Converter

Instrument in STORE mode at 0.5ms/cm

Test Point	Signal (TTL logic levels unless otherwise specified)
U834 pin 11	200kHz clock
U819 pin 11	200kHz clock
U820 pin 13	+6.2V
U827a pin 1	3.9V D.C. level Sensitivity 70mV/cm
U827d pin 14	3.9V D.C. level Sensitivity 70mV/cm

(l) Digital Ramp Generator

Instrument in STORE mode at 0.5ms/cm

Test Point	Signal
U831 pin 23	200Hz clock with even mark/space
U825a pin 1	200Hz ramp from 0V to 3.5V
U830a pin 8	200kHz clock with even mark/space
U830a pin 5	200Hz ramp from 0V to 3.5V

5.4 SETTING UP PROCEDURE

The following procedure details the adjustments necessary to recalibrate the OS1420 and set all the preset controls to achieve the specified performance. Inability to make these adjustments or failure to meet the specification after those adjustments have been made should be considered as a fault and the operating conditions should be checked according to section 5.3.

Set instrument initially in NORMAL mode.

a. Test Equipment

1. Multirange Test Meter including 2.5kV capability at 20kΩ/V.
2. Variable Autotransformer, output voltage 100-170V at 5A.
3. Sine/square wave signal generator, 10Hz to 100kHz, 20mV –5V.
4. Source of voltage and time calibration signals, such as Bradley Oscilloscope Calibrator type 192.
5. Square wave generator, 500kHz, 100mV into 50Ω, rise time less than 50ns with square corner and flat top.
6. RF Sinewave, Constant Amptitude Signal Generator. 25mV to 5V pk/pk 50kHz to 15MHz.
7. 10:1 passive probe (PB12 or PB13).

b. Set E.H.T.

Set the incoming a.c. supply via the auto-transformer to the nominal centre voltage of the selected range. Set to mid brilliance on the c.r.t. Monitor the collector voltage of TR707. Adjust R725 for this voltage to be +405V +5V. Remove the voltmeter. The instrument may now be operated directly from the uncontrolled supply.

c. Set Intensity Range

Set to X-Y mode with inputs grounded and centre the spot on the screen. Monitor the collector voltage of TR702. Adjust the intensity control for this voltage to be +15V and then adjust R713 for the intensity of the spot to be near cut off. Remove the voltmeter.

d. Astigmatism

Display a mid-frequency sinusoidal signal in the normal sweep mode on one channel, approx 2cm pk. to pk and 4cm period. Set the Variable sensitivity control fully anticlockwise. Set to a fairly low brilliance and adjust both the Focus control and R708 (Astig.) for the sharpest trace over the whole of its length. Reset the Variable sensitivity to Cal.

e. Trace Rotation

Ground the input and set the horizontal trace to the centre line. Adjust the Trace Rotation preset control to align the trace with the centre graticule line.

f. Input Balance

Select CH1 and with the input grounded, adjust the preset Bal. control for no vertical movement of the trace between the 0.1V/cm and the 0.2V/cm ranges. Repeat for CH2.

g. Trigger Balance

Set R357 for no vertical movement of the channel 2 trace when Invert is selected. Connect a sinusoidal input, AC coupled, to CH1 and set the trace for about 5cm pk. to pk. signal and one cycle displayed Adjust R307 such that there is no change of trigger point as the Trigger Coupling is switched between AC and DC. Note that the relevant shift control may have to be operated to return the trace to the centre of the screen when R357 or R307 are adjusted;

h. Timebase Calibration

Ensure that the Variable Sweep is set fully clockwise to Cal. Apply 0.1ms calibrated time markers to either channel input. Set the timebase to 0.1ms/cm and obtain a centred triggered trace. Apply X10 Magnification and set R553 for 10cm spacing between the time markers.

Return to X1 Magnification and set R551 for 1cm spacing between markers.

Apply 1ms/cm time markers and set the timebase to 1ms/cm. Set R506 for 1cm spacing between the time markers.

All other timebase ranges can be checked for accuracy.

i. X-Y Calibration

Ensure that the CH1 Variable Sensitivity control is set fully clockwise to Cal. Select X-Y and apply a calibrated 100mV square wave to Channel 1 input. Select 20mV/cm Ground Channel 2. Set R302 for 5cm horizontal trace length.

j. Channel 1 Calibration

Select CH1. With 100mV input at 20mV/cm as i. above, set R415 for a 5cm vertical amplitude signal.

All other sensitivity ranges can be checked for accuracy.

k. Ensure that the CH2 Variable Sensitivity control is set fully clockwise to Cal. Transfer the 100mV calibration signal to channel 2 and set to display that channel at 20mV/cm. Set R352 for a 5cm vertical amplitude signal.

All other sensitivity ranges can be checked for accuracy.

l. Attenuator Compensation

Apply a square wave input to CH1 at approx. 1V pk. to pk. and 1kHz. Select 0.2V/cm and adjust C101 on the CH1 attenuator assembly to obtain a square-topped displayed pulse. Access is through the screw driver/trim tool hole in the pre-amplifier board.

Repeat for CH2.

m. Input Capacitance Equalisation

Select 100mV/cm on CH1 with the Variable Sensitivity control set fully anticlockwise and monitor a 10V 1kHz square wave via a 10:1 probe. Adjust the capacitive compensation of the probe for a flat-topped displayed pulse. Select 200mV/cm, reset the Variable Sensitivity to Cal and adjust C102 for a similar flat top to the pulse. Access is through the screw driver/trim Tool Hole in the pre-amplifier board.

Repeat for Channel 2.

n. Pulse Response and Bandwidth

Monitor a fast rise square wave input signal to examine the edge in detail on the 20mV/cm and 0.5μs/cm ranges.

Adjust C405 for a flat top following the transition and C402 for the optimum corner to the pulse.

Connect a constant amplitude sinusoidal generator and set the input for 5cm pk. to pk. at 50kHz. Increase the frequency and check that the loss of amplitude is less than 3dB at 20MHz (3.5cm pk. to pk.).

o. Calibrator

Monitor a calibrated 1V pk. to pk. square wave input and set the sensitivity and variable sensitivity controls for a full 8cm pk. to pk. display. Disconnect the external input and connect the Y input to the OS1420 Calibrator output. Adjust R641 for a similar 8cm signal amplitude.

p. Adjustment of the Y D.A.C. output.

Apply a 100mV square wave input to CH1 and set the CH1 attenuator to 10mV/cm. Set STORE mode, and operate the RELEASE control with the TIME/CM switch set to 0.5ms/cm. Adjust R829 to centre the display on the screen. Adjust R821 so that the upper and lower levels of the display are just on screen at both the upper and lower edge of the screen.

q. Adjustment of the A.D.C.

Select STORE mode, CH1 input coupling to DC, TIME/CM switch to 0.5ms/cm, and set DISPLAY MODE switch to CH1. Apply a 100mV/cm signal to CH1 and select 20mV/cm on the attenuators. Adjust R842 so that the display waveform is 5cm in amplitude.

r. Adjustment of pickoff board

Set CH1 input coupling switch to GND. Ensure CH1 trigger is selected and BRIGHT LINE is On. Set NORMAL mode, and 0.5ms/cm on the TIME/CM switch. Adjust the CH1 Y shift control to centre the trace on the display. Switch to STORE mode. If a trace displacement occurs, adjust R1325 to bring the trace back to the centre of the screen. Switch back to NORMAL mode and display TRACE to the upper edge of the screen. Return back to STORE mode and adjust R1323 set the trace at the upper edge of the screen, if necessary.

s. Digital Timebase adjustment

Apply 1ms markers to CH1 input. Set the TIME/CM switch to 0.1ms. Select STORE mode and operate the RELEASE button. Obtain a centred triggered trace and adjust R834 to obtain 1cm spacing between the markers.

NOTE TO SECTION 5.4

The unstabilised EHT voltage is a function of the peak-to-peak supply voltage and is thus waveform dependent. Operation of the set via a variable or other transformer may introduce peak clipping of the supply to the set and cause subsequent errors in checking or re-setting the EHT stabiliser range. (R725 according to section 5.4b above).

To check the effect of introducing a variable transformer to drive the set, first operate the set directly from the supply and note the supply voltage and the collector voltage of TR707.

Then operate the set via the variable transformer and adjust the supply voltage to the set to give the same voltage on TR707. Any difference in the supply voltage as measured represents a limitation of the variable transformer.

For example:-
Assume that when operating directly from the supply, the supply is measured as 250V and the voltage on TR707 as 430V.

Then on operation of the set through a variable transformer, the output of that transformer into the set is measured as 265V when adjusted to give the same 430V on TR707. The difference of 15V is a result of the impedance of the variable transformer. The input to the set should be adjusted to 240V + 15V, (i.e. 255V) to check or set the voltage on TR707 to 405V.

The voltage on TR707 can have an error of ± 20V before any stabilisation problem occurs. Note that adjustment of R725 changes the stabilised EHT voltage and subsequent full recalibration of the set is required. The stabilised EHT voltage should be −1850V ±5%.

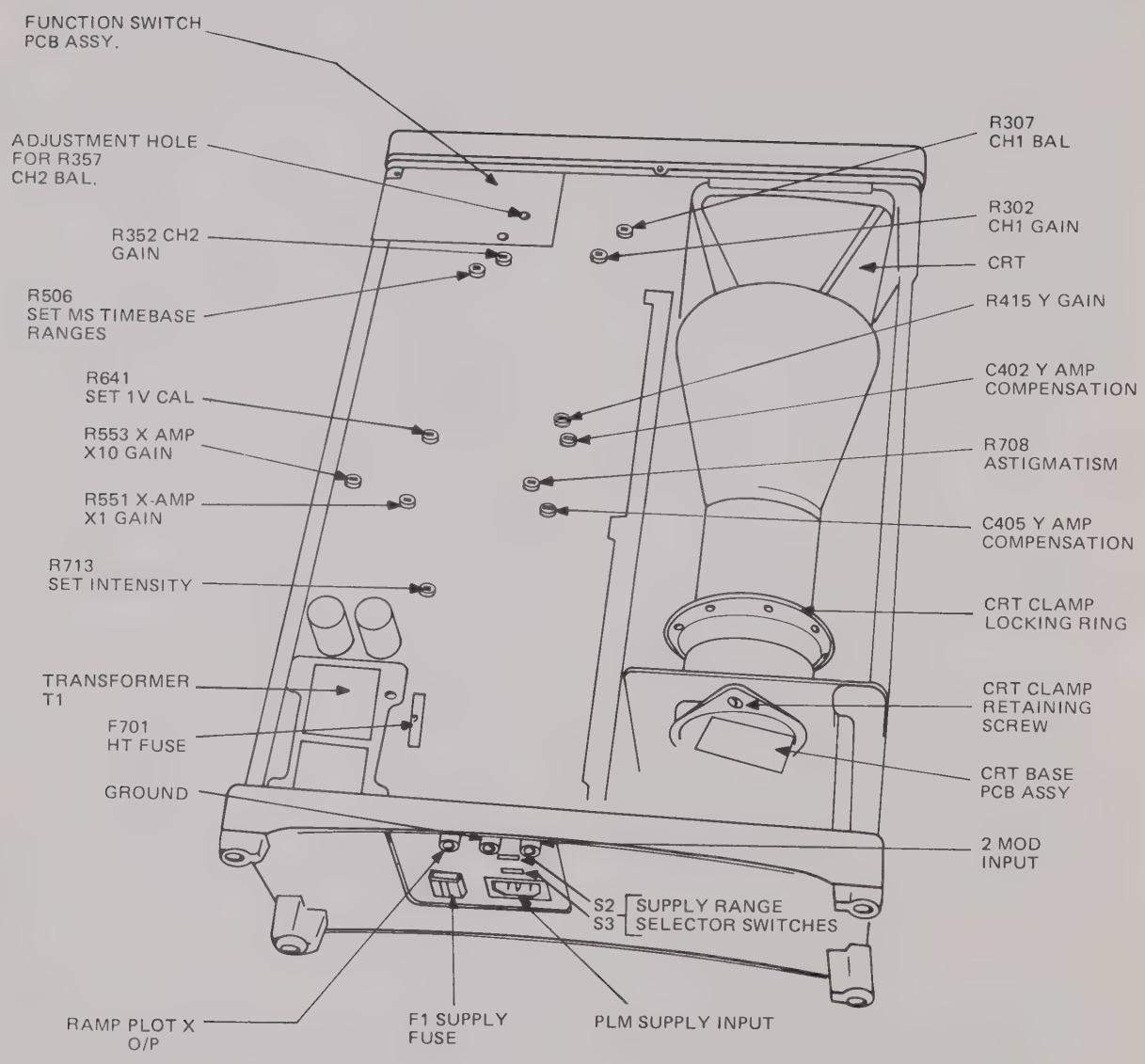


Fig. 2 Internal Assembly – Top View

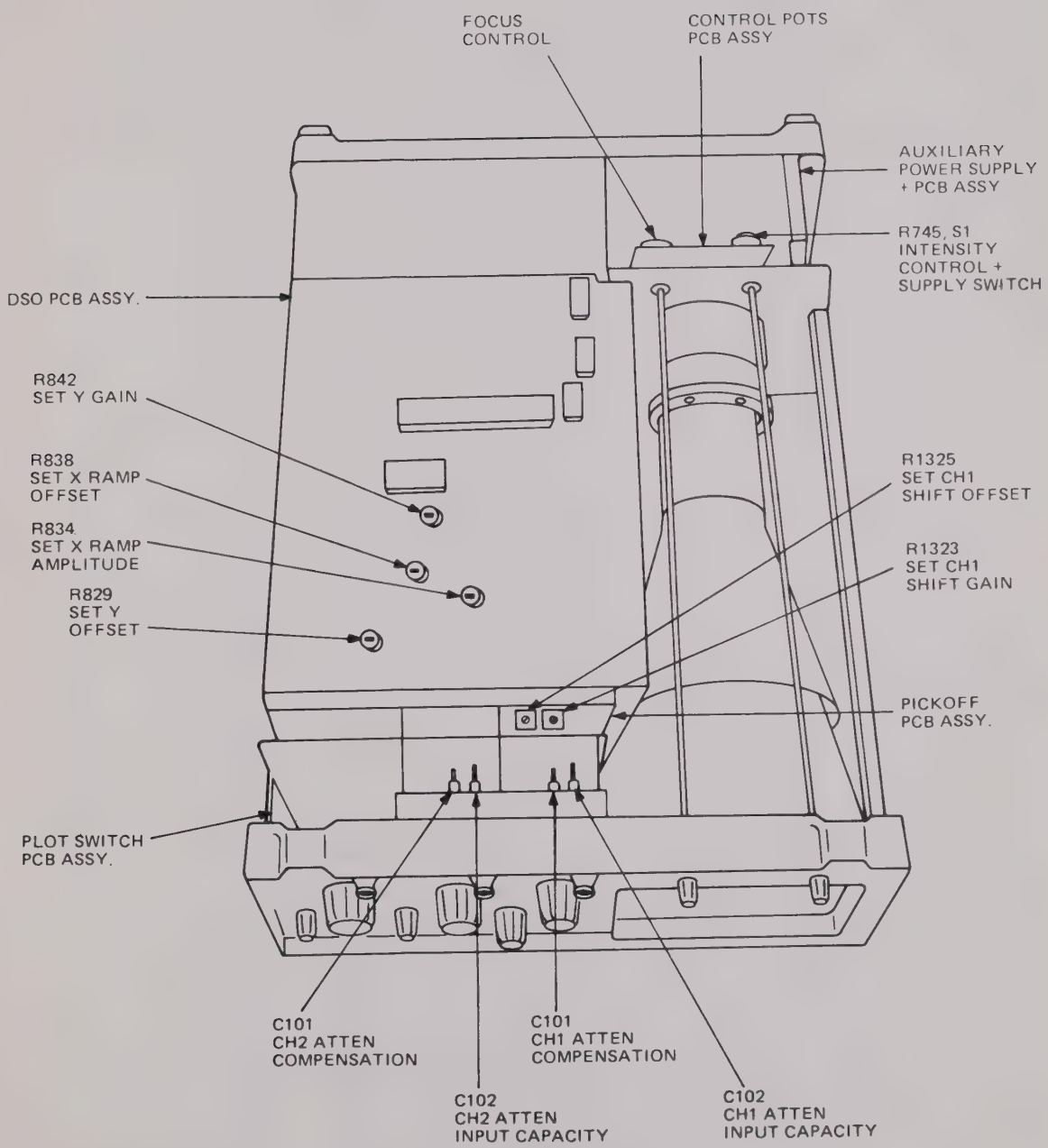

FOCUS CONTROL
CONTROL POTS PCB ASSY
AUXILIARY POWER SUPPLY + PCB ASSY
R745, S1 INTENSITY CONTROL + SUPPLY SWITCH
DSO PCB ASSY.
R842 SET Y GAIN
R838 SET X RAMP OFFSET
R834 SET X RAMP AMPLITUDE
R829 SET Y OFFSET
R1325 SET CH1 SHIFT OFFSET
R1323 SET CH1 SHIFT GAIN
PICKOFF PCB ASSY.
PLOT SWITCH PCB ASSY.
C101 CH2 ATTEN COMPENSATION
C101 CH1 ATTEN COMPENSATION
C102 CH2 ATTEN INPUT CAPACITY
C102 CH1 ATTEN INPUT CAPACITY

Fig. 3 Internal Assembly – Bottom View

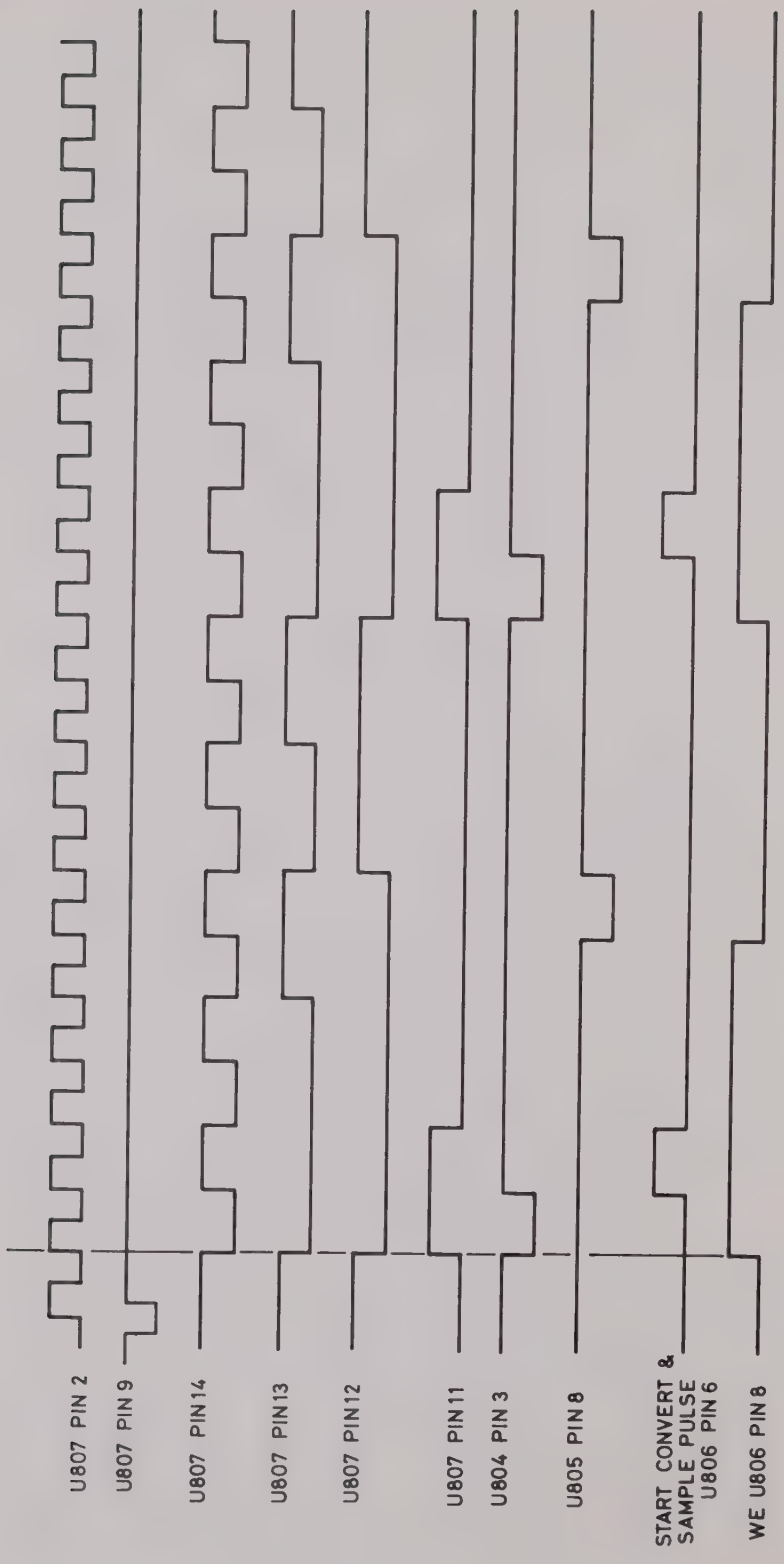


Fig. 4 Control & Timing Logic Waveforms

TIME / CM 0·5 mS / CM
WRITE ADDRESS INCREMENTS
LATCH READ DATA
(DAC & READ ADDR. INCREMENTS)
RW CLK. U831 PIN 48
WRITE ADDR.
READ ADDR.
NMWE U831 PIN 27
IN ROLL MODE WHEN WRITE ADDRESS INCREMENTS THE NEXT READ ADDRESS INCREMENTS BY TWO.

Fig. 5 Store Control Waveforms

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	¼W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potenitometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
CE(3)	Ceramic	50V		unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

OS1400 INTERCONNECTIONS DIAGRAM

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1101	1k	CF			21799
R1102	390	CF			28722
R1103	4k7	CF			21805
R1104	10k	CF			21809
R1105	10k	CF			21809
R1106	270k	CF			32356
R1107	330k	CF			32357
R1108	470k	CF			32330
R1109	4k7	CF			21805
R1110	100k	CF			21819
R1111	10k	CF			21809
CAPACITORS					
C1101	10nF	CE(3)		25V	450548
C1102	10nF	CE(3)		25V	450548
C1103	10nF	CE(3)		25V	450548
C1104	470nF	CE(3)			43500
C1105	100nF	CE(3)			43498
DIODES					
D1101					43847
Q1101		MPS2369			36625
U1101		74C221			451267
U1102		ICM7555IPA			451317
MISCELLANEOUS					
S1101 –1106					450750
S1401 S1404					450992

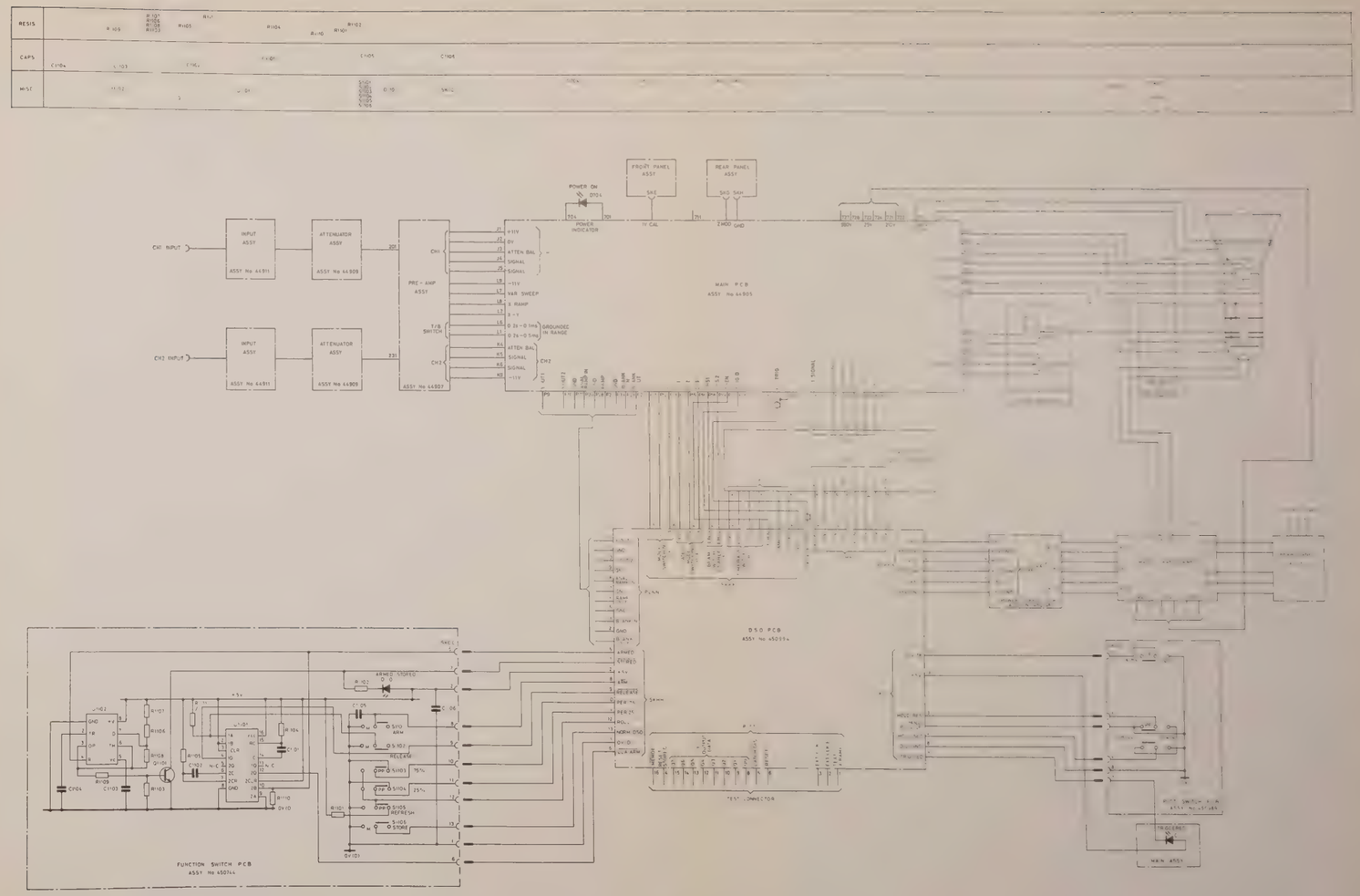


Fig. 6 Interconnection Diagram

OS1400 Y AMP, TIMEBASE & TRIGGER

RESISTORS

Ref	Value	Description	Tol %±	Rating	Part No
R1	47	CF			28714
R2	47	CF			28714
R101	27	CF			28711
R103	22	CF			28710
R133	22	CF			28710
R151	82k	CF		1W	19060
R201	1k8	CF			28725
R202	10	CF			21793
R204	1k5	CF			21801
R205	3k3	CF			21803
R206	47	CF			28714
R207	470k	CC			4906
R208	150	CF			28719
R210	820	CF			28724
R211	510	CF			29434
R212	820	MF	2		38592
R213	820	MF	2		38592
R214	1k5	MF	2		38598
R215	1k5	MF	2		38598
R216	180	CF			21795
R217	4k7	CP			451368
R231	1k8	CF			28725
R232	10	CF			21793
R234	1k5	CF			21801
R235	10k	CF			21809
R236	47	CF			28714
R237	470k	CC			4906
R238	150	CF			28719
R240	820	CF			28724
R241	510	CF			29434
R242	820	MF	2		38592
R243	820	MF	2		38592
R244	1k5	MF	2		38598
R245	1k5	MF	2		38598
R246	180	CF			21795
R247	4k7	CP			451368
R261	10	CF			21793
R262	470	CF			21797
R263	4k7	CF			21805
R265	1k	CF			21799
R266	1k	CF			21799
R267	10	CF			21793
R268	100	CF			21794
R269	47k	CP			A3/451367
R270	4k7	CP			A3/451369
R271	2k2	CP			451370
R272	47k	CF		1/8W	44242
R273	8k2	CF		1/8W	44234
R274	2k2	CP			451370
R301	10k	PCP			44959
R302	220	PCP			36262
R306	1k	CF			21799
R307	10k	PCP			36267
R308	22k	CF			21812
R309	120	CF	2		38572
R311	10	CF			21793
R312	10	CF			21793
R313	100	CF			21794
R314	100	CF			21794
R315	4k7	CP			A3/451371
R316	3k3	MF	2		38606
R317	3k3	MF	2		38606
R318	7k5	CF			40297
R319	7k5	CF			40297
R351	10k	PCP			44959
R352	220	PCP			36262
R356	1k	CF			21799
R357	10k	PCP			36267
R358	22k	CF			21812
R359	120	MF	2		38572
R361	10	CF			21793
R362	10	CF			21793
R363	100	CF			21794
R364	100	CF			21794
R365	4k7	CP			A3/451371
R366	3k3	MF	2		38606
R367	3k3	MF	2		38606
R368	7k5	CF			40297
R369	7k5	CF			40297
R371	330	CF			28721
R372	330	CF			28721
R401	2k2	MF	2		38602
R402	2k2	MF	2		38602
R403	2k2	CF			21802
R404	2k2	CF			21802
R405	2k7	MF			38604
R406	47	CF			28714
R407	2k7	MF	2		38604
R408	1k5	CF			21801
R409	1k5	CF			21801
R410	1k8	CF			28725
R411	1k8	CF			18553
R412	390	MF	2		38584
R413	1k8	CF		½W	18553
R414	390	MF	2		38584
R415	100	PCP			36261
R416	47	CF			28714
R417	150	MF	2		38574

OS1400 Y AMP. TIMEBASE & TRIGGER (Cont.)

RESISTORS (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
R418	270	MO			26742
R419	10	CF			21793
R421	10	CF			21793
R422	270	MO			26742
R423	150	CF			28719
R424		A.O.T.			
R425	100	MF	2		38570
R426	120	CF			28718
R427	120	CF			28718
R428	22	CF			28710
R429	39k	CF		1W	19056
R432	22	CF			28710
R433	47	CF			28714
R434	47	CF	5		28714
R437	100	CF			21794
R438	100	CF			21794
R439	270	CF		1W	19036
R440	270	CF		1W	19036
R441	270	CF		1W	19036
R442	2k2	MO	5		44986
R443	2k2	MO	5		44986
R444	47	CF			28714
R445	47	CF			28714
R503	470	CF			21797
R504	56k	CF			28729
R505	27k	CF			21813
R506	10k	PCP			36267
R507	4k7	CF			21805
R508	4k7	CF			21805
R509	33k	CF			21814
R510	10	CF			21793
R511	10k	CF			21809
R512	33k	CF			21814
R515	5k6	CF			21806
R514	1k5	CF			21801
R515	1k5	CF			21801
R516	1k	CF			21799
R517	22k	CF			21812
R518	22k	CF			21812
R519	3k9	CF			21804
R520	10k	CF			21809
R521	1k	CF			21799
R522	2k2	CF			21802
R523	4k7	CF			21805
R524	3k9	CF			21804
R525	2k2	CF			21804
R526	3k9	CF			21802
R527	680	CF			28723
R528	680	CF			28723
R529	1k	CF			21799
R530	56	CF			28715
R532	180	CF			21795
R533	1k2	CF			21800
R534	6k8	CF			21807
R535	680	CF			28723
R536	10	CF			21793
R537	10	CF			21793
R538	10	CF			21793
R539	470	CF			21797
R541	1k8	CF			28725
R542	47	CF			28714
R544	470	CF			21797
R545	2k7	CF	A.O.T.		28726
R546	6k8	CF			21807
R547	2k2	CF			21802
R548	8k2	CF			21808
R549	6k8	CF			21807
R551	1k	PCP			36264
R552	5k6	CF			21806
R553	4k7	PCP			36266
R554	680	CF			28723
R555	47	CF			28714
R556	2k7	CF			28726
R557	1k8	CF			28725
R558	10	CF			21793
R559	100	CF			21794
R560	68k	CF			21816
R561	100	CF			21794
R562	10k	CF			21809
R563	390	CF		½W	18545
R564	33k	CF			21814
R565	2k2	CF			21802
R566	100k	MO			28822
R567	390	CF		½W	18545
R568	22k	CF			21812
R569	510	MF	2		38587
R570	15k	CF	A.O.T.		28727
R571	820	CF			28724
R572	22k	CF			21812
R573	4k7	CF			21805
R574	12k	CF		1W	19051
R575	12k	CF		1W	19051
R576	10k	MO	5		44987
R577	10k	MO	5		44987
R600	22k	CF			21812
R601	27k	CF			21813
R603	3k3	CF			21803
R604	4k7	CF			21805
R605	2k2	CF			21802
R606	27k	CF			21813
R607	2k2	CF			21802

OS1400 Y AMP, TIMEBASE & TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R608	4k7	CF			21805
R609	470	CF			21797
R610	10	CF			21793
R611	680	CF			28723
R612	680	CF			28723
R613	68k	CF			21816
R614	10	CF			21793
R615	12k	CF			21810
R616	470	CF			21797
R617	2k7	CF			28726
R618	47k	CF			21815
R619	3k3	CF			21803
R620	1M	CF			31840
R621	3k3	MF			21803
R622	1k8	CF			28725
R623	220k	CF			21823
R624	10	CF			21793
R625	1M	CF			31840
R626	1M	CF			31840
R627	680k	CF			31839
R628	1M	CF			31840
R629	1M	CF			31840
R630	100k	CF			21819
R631	33k	CF			21814
R632	300k	MF	2		38653
R633	18k	CF			21811
R634	6k8	CF			21807
R635	10	CF			21793
R636	68k	CF			21816
R637	2k2	CF			21802
R638	3k9	CF			21804
R639	10k	CF			21809
R640	39k	CF			28728
R641	2k2	PCP			36265
R642	56k	CF		½W	19058
R643	470	CF			21797
R644	3k3	CF			21803
R645	10k	CF			21809
RN101		RESISTOR NETWORK			A3/43194
RN201		RESISTOR NETWORK			A3/44651
RN231		RESISTOR NETWORK			A3/44651
RN261		RESISTOR NETWORK			A3/38692
CAPACITORS					
C101	1/6pF	TRIMMER			450510
C102	1/6pF	TRIMMER			450510
C103		A.O.T.			
C104	680pF	PC			40631
C105	100nF	CE(2)		400V	44966
C106	6.8pF	CE(2)			22362
C133		A.O.T.			
C135	100nF	PE			400V 44966
C151	6.8pF	SM			500V 22362
C201	10µF	E			25V 32180
C202	2.2nF	CE(2)			22389
C204	1nF	CE(3)			42432
C231	10µF	E			25V 32180
C232	10nF	CE(3)			25V 450548
C233	2.2nF	CE(2)			22389
C234	1nF	CE(3)			42432
C237	10nF	CE(3)			25V 450548
C263	12nF	PS			63V 450536
C264	1µF	PE			100V 41743
C265	10nF	CE(3)			25V 450548
C266	10nF	CE(2)			100V 37018
C267	10nF	CE(3)			25V 450548
C268	10nF	CE(3)			25V 450548
C301	10nF	CE(3)			25V 450548
C302	10nF	CE(3)			25V 450548
C351	10nF	CE(3)			25V 450548
C352	10nF	CE(3)			25V 450548
C401	10nF	CE(3)			25V 450548
C402	10/65pF	TRIMMER			30286
C403	15pF	CE(3)			42410
C404	82pF	CE(3)			42419
C405	1065/pF	TRIMMER			30286
C406		A.O.T.			
C407	100nF	CE(2)			100V 37018
C408	3.3nF	CE(3)			42438
C409	3.3nF	CE(3)			42438
C411	5.6nF	CE(2)			500V 22394
C412	15pF	CE(3)	A.O.T.		42410
C413	1nF	CE(3)			50V 42432
C501	220nF	PE			100V 44370
C502	1nF				42432
C503	10nF	CE(3)			25V 450548
C504	10nF	CE(3)			25V 450548
C506	10pF	CE(3)			42408
C507	10nF	CE(3)			25V 450548
C508	10nF	CE(3)			25V 450548
C509	100µF	E			16V 450582
C510	560pF	CE(3)			42429
C511	3.3nF	CE(3)			42438

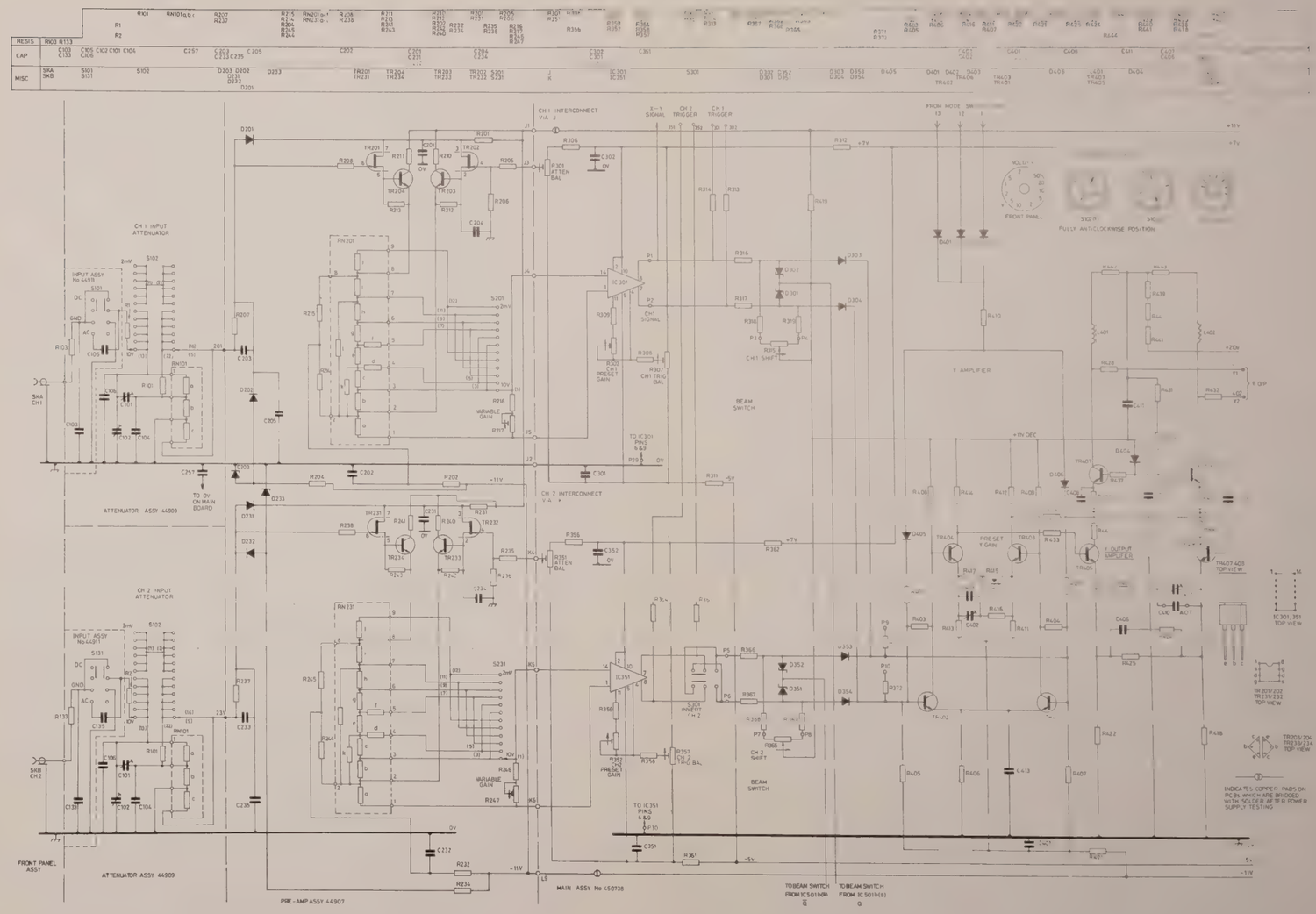


Fig. 7 Y Amplifier Circuit Diagram

OS1400 Y AMP, TIMEBASE & TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C512	6.5nF	CE(2)			22394
C513	100µF	E		16V	450582
C514	120pF	CE(3)			42421
C515	150pF	CE(3)			42422
C516	150pF	CE(3)			42422
C520	10µF	E		25V	32180
C601	220nF	PE		250V	39201
C602	100pF	CE(3)			42420
C603	2.2µF	E		63V	32194
C604	2.2µF	E		100V	450593
C605	22pF	CE(3)			42412
C606	100nF	CE(2)		100V	37018
C607	100nF	CE(2)		100V	37018
C608	220nF	PE		100V	44370
C609	100nF	CE(2)		100V	37018
C610	10nF	CE(3)		25V	450548
C611	22pF	CE(3)			42412
C612	100nF	CE(2)		100V	37018
C613	10nF	CE(3)		25V	450548
C614	47pF	CE(3)			42416
C615	100nF	CE(2)		100V	37018
C616	10nF	CE(3)		25V	450548
C617	47nF	CE(2)		100V	39192
C618	47nF	CE(2)		100V	39192
C619	100pF	CE(3)			42420
C620	10nF	CE(3)		25V	450548
C621	10nF	CE(3)		25V	450548
C622	2.2µF	E			32194
C623	3.3pF	CE(3)			36600
C701	10nF	CE(3)		25V	450548
C702	2.2nF	PE		4kV	A4/44990
C703	2.2nF	PE		4kV	A4/44990
C704	1000µF	E		40V	44992
C705	33µF	E		350V	44991
C708	10µF	E		25V	32180
C709	2.2nF	PE		4kV	A4/44990
C710	10µF	E		25V	32180
C711	100nF	PE		1.5kV	40075
C712	100nF	PE		1.5kV	40075
C713	220nF	PE		100V	44370
C714	10nF	CE(3)		25V	450548
C715	220nF	PE		100V	44370
C716	10nF	CE(3)		25V	450548
C717	56pF	CE(3)			42417
C718	22pF	CE(3)	A.O.T.		42412
C719	5.6nF	CE(2)			22394
TRANSISTORS					
TR201, TR202		DUAL F.E.T.			44704
TR203, TR204		AE38			44627
TR231, TR232		DUAL F.E.T.			44704
TR233, TR234		AE38			44627
TR261		ZTX313			40788
TR262		BC547B			44951
TR263		BC558C			44952
TR264		BC558C			44952
TR401		BF371			36275
TR402		BF371			36275
TR403		BF371			36275
TR404		BF371			36275
TR405		ZTX313			40788
TR406		ZTX313			40788
TR407		BF468			40056
TR408		BF468			40056
TR501		BC547B			44951
TR502		MPS2369			36625
TR503		MPS2369			36625
TR504		BC547B			44951
TR505		2N3904			24146
TR506		BC558C			44592
TR507		BC557B			44590
TR508		BC557B			44950
TR509		BC547B			44951
TR511		2N3904			24146
TR512		2N3906			21533
TR513		NSD459			40054
TR514		NSD459			40054
TR515		BF393			450226
TR601		BC558C			44952
TR602		BC558C			44952
TR603		BC547B			44951
TR605		BC557B			44950
TR605		2N3904			24146
TR606		2N3904			14146
TR607		2N3906			21533
TR701		TJ630			44953
TR702		BFR86B			44954
TR703		BFR86B			44954
TR704		BC558C			44952
TR706		BC547B			44951
TR707		BUX87			44955
TR709		BC328			38414
TR711		BC558C			44952
TR712		TIP29A			38419
TR713		TIP112			40591

OS1400 Y AMP, TIMEBASE & TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
TRANSISTORS (Cont.)					
TR714		BC547B			44951
TR715		BC557B			44950
TR716		2N6518			36472
DIODES					
D201		IN3595			29330
D202		IN3593			29330
D203	6V8	ZENER			33931
D231		IN3595			29330
D232		IN3595			29330
D233	6V8	ZENER			33931
D301		ZC2811H			40352
D302		ZC2811H			40352
D303		IN4148			34701
D304		IN4148			34701
D351		ZC2811H			40352
D352		ZC2811H			40352
D353		IN4148			34701
D354		IN4148			34701
D401		IN4148			23802
D402		IN4148			23802
D403		IN4148			23802
D404	5V1	ZENER			33928
D405		IN4148			34701
D406		IN4148			34701
D501		IN4148			23802
D502		OA47			4468
D503		IN4148			23802
D504		IN4148			23802
D505		IN4148			23802
D506		IN4148			23802
D507		IN4148			23802
D508		IN4148			23802
D509		IN4148			23802
D510		IN4148			23802
D511		IN4148			23802
D512		IN4148			23802
D513		IN4148			23802
D514		IN4148			23802
D515		IN4148			23802
D516		IN4148			23802
D517		IN4148			23802
D518		IN4148			23802
D519		IN4148			23802
D520		IN4148			23802
D521	6V2	ZENER			33930
D522		IN4148			23802
D523		IN4148			23802
D524		ZC2811H			40352
D525		ZC2811H			40352

Ref	Value	Description	Tol %±	Rating	Part No
D601		IN4148			23802
D602		IN4148			23802
D603		IN4148			23802
D604		IN4148			23802
D605	5V6	ZENER			33929
D606		IN4148			23802
D607		IN4148			23802
D608		IN4148			23802
D609	47V	ZENER			40049
D610		IN4148			23802
D611		IN4148			23802
INTEGRATED CIRCUITS					
IC261		LF351			40130
IC301		LM733CN			40084
IC351		LM733CN			40084
IC501		74LS74N			36732
IC552		LM78L05 ACZ			40406
IC601		MC3401P			40061
IC602		LM710CN			40083
IC701		MC78L12 ACP			40060
IC702		LM341P15			40059
MISCELLANEOUS					
L401	15μH				44993
L402	15μH				44993
S1		WITH R745			A4/44461
S2					A4/4069
S3					A4/4069
S101					A4/44965
S102					44978
S131					A4/44965
S201					450294
S231					450294
S261					A4/44476
S262					A4/450760
S301					A4/38729
S501 –506 S507					A4/38728 A4/38729

OS1400 Y AMP, TIMEBASE & TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
MISCELLANEOUS (Cont.)					
SKA					1222
SKB					1222
SKC					1222
SKD					37293
SKE					31229
F1	250mA	FOR 250V SUPPLY			33684
	500mA	FOR 110V SUPPLY			33685

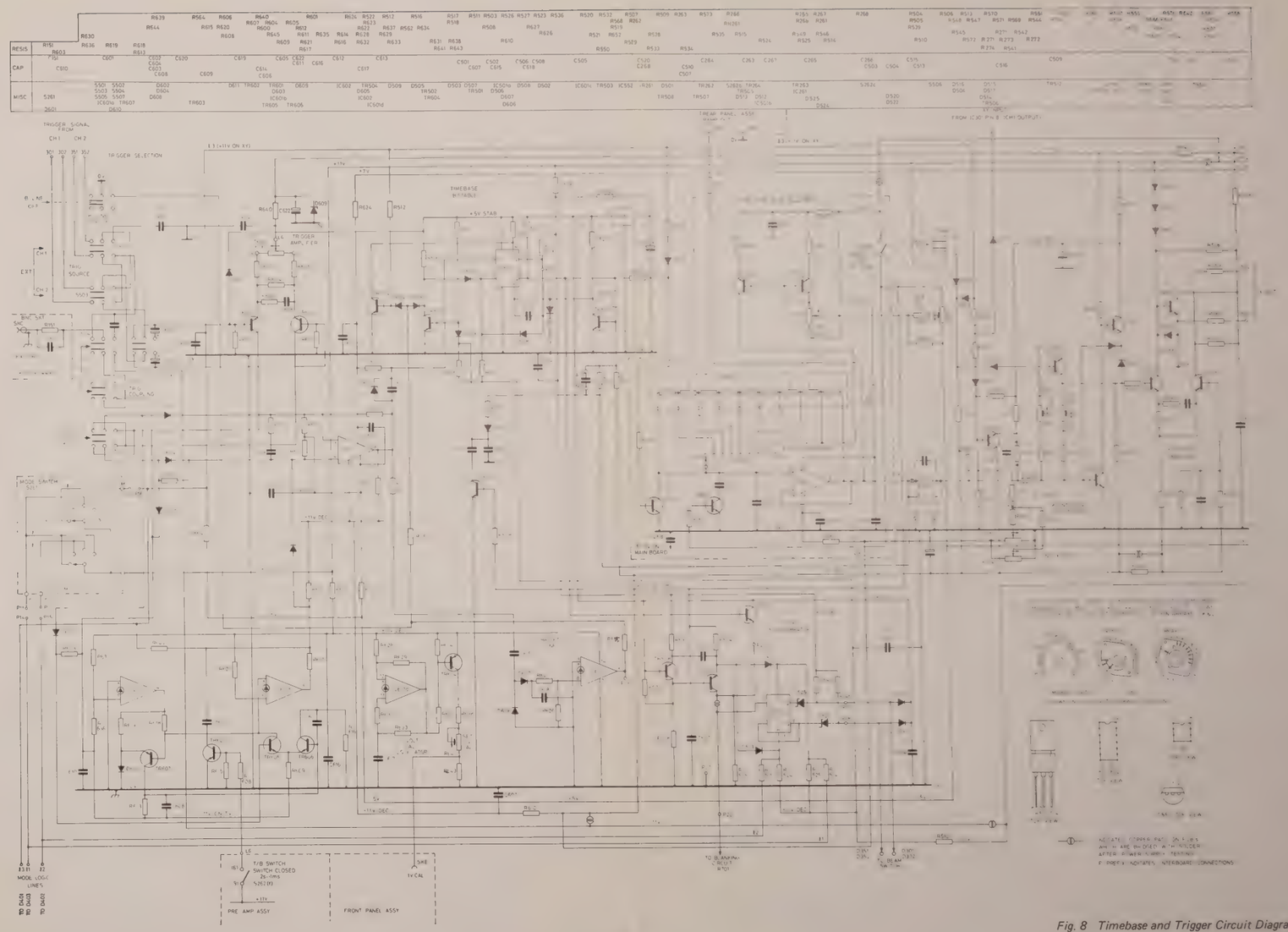
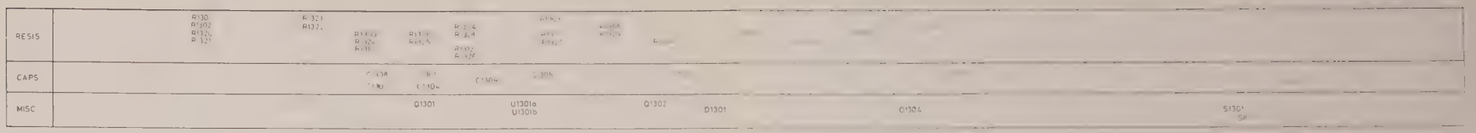
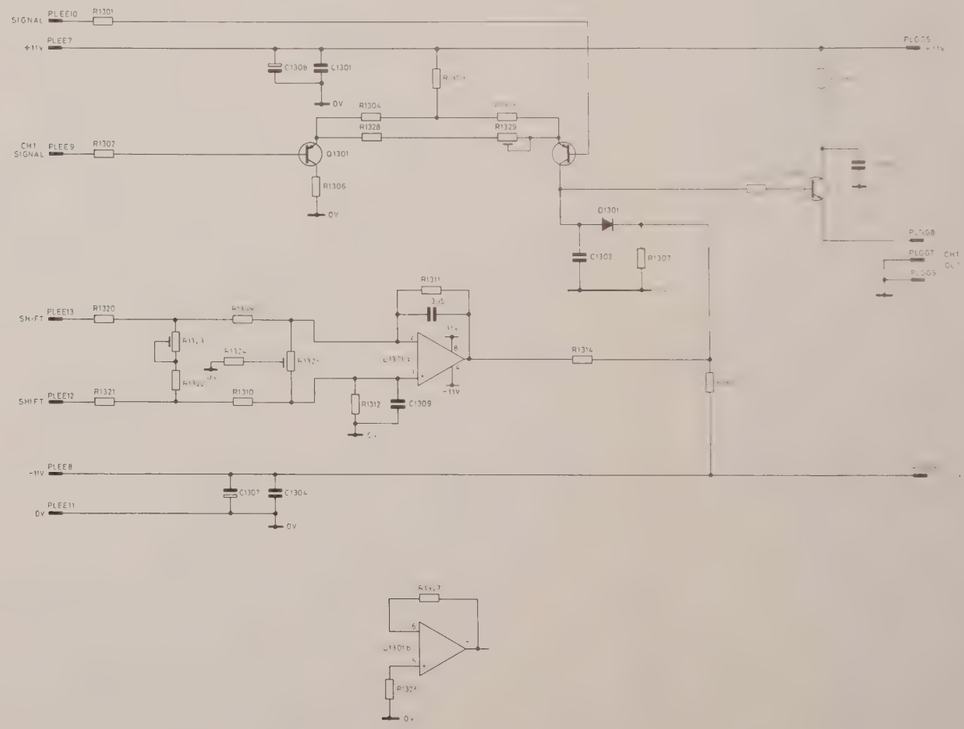


Fig. 8 Timebase and Trigger Circuit Diagram

OS1400 PICK-OFF CIRCUIT

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1301	47	CF			28714
R1302	47	CF			28714
R1303	1K	CF			21799
R1304	220	CF			21796
R1305	220	CF			21796
R1306	270	CF			28720
R1307	270	CF			28720
R1309	15k	CF			28727
R1310	15k	CF			28727
R1311	100k	CF			21819
R1312	100k	CF			21819
R1314	1k5	CF			21801
R1316	3k3	CF			21803
R1317	47	CF			28714
R1318	220	CF			21796
R1319	1k5	CF			21801
R1320	18k	CF			21811
R1321	18k	CF			21811
R1322	22k	CF			21812
R1323	47k	CP			42166
R1324	220k	CF			21823
R1325	100k	CP			42167
R1326	100k	CF			21819
R1327	100k	CF			21819
R1328	470	CF			21797
R1329	1k	PCP			35898
CAPACITORS					
C1301	10nF	CE(3)		25V	450548
C1302	270pF	CE(3)			42425
C1304	10nF	CE(3)		25V	450548
C1305	100nF	CE(3)			43498
C1306	10nF	CE(3)		25V	450548
C1307	10µF	E		25V	32180
C1308	10µF	E		25V	32180
C1309	100nF	CE(3)			43498
C1310	10nF	CE(3)		25V	450548
Q1301		2N5771			38089
Q1302		2N5771			38089
Q1304		MPS2369			36625
DIODES					
D1301		IN4148			23802
MISCELLANEOUS					
S1301					A4/450761
PLEE		Molex wafer			451534
SKFF					38001





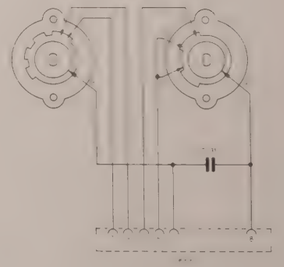


Fig. 9 Pickoff Circuit Diagram

OS1400 D.S.O. CIRCUIT

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R801	100	CF			21794
R802	10k	CF			21809
R803	2k2	CF			21802
R804	47	CF			28714
R805	5k6	CF			21806
R806	330	CF			28721
R807	1k8	CF			28725
R808	100	CF			21794
R809	1k	CF			21799
R810	1k	CF			21799
R811	390	CF			28722
R812	10	CF			21793
R813	10	CF			21793
R814	100	CF			21794
R815	47	CF			28714
R816	820	CF			28724
R817	5k6	CF			21806
R818	1k5	CF			21801
R819	3k9	CF			21804
R820	6k8	CF			21807
R821	10k	CP			36267
R822	180	CF			21795
R823	3k	MF			38605
R824	3k	MF			38605
R825	3k9	CF			21804
R826	3k9	CF			21804
R827	5k6	CF			21806
R828	5k6	CF			21806
R829	470	CP			36263
R830	220	MO	2		38578
R831	220	MO	2		38578
R832	100	CF			21794
R833	820	CF			28724
R834	470	CP			36263
R835	1k5	CF			21801
R836	1k5	CF			21801
R837	18k	CF			21811
R838	10k	CP			36267
R839	18k	CF			21811
R840	560	CF			21798
R841	5k6	CF			21806
R842	220	CP			36262
R843	390	CF			28722
R844	6k2	MF	2		38613
R845	6k2	MF	2		38613
R846	6k2	MF	2		38613
R847	6k2	MF	2		38589
R848	18k	CF			21811
R849	22k	CF			21812
R850	100k	CF			21819
R851	330	CF			28721
R852	100k	CF			21819
R853	18k	CF			21811
R854	330	CF			28721
R856	22k	CF			21812
R857	22k	CF			21812
R858	22k	CF			21812
R859	22k	CF			21812
R860	5k6	CF			21806
R861	22k	CF			21812
R862	4k7	CF			21805
R863	15k	CF			28727
R864	15k	CF			28727
R865	4k7	CF			21805
R866	4k7	CF			21805
R867	680	CF			28723
R868	680	CF			28723
R869	18k	CF			21811
R871	220	CF			21796
R872	47k	CF			21815
R873	1k	CF			21799
R874	47k	CF			21815
R880	100	CF			21794
R881	15k	MO	2		38622
R882	15k	MO	2		38622
R883	7k5	MF	2		38615
R884	7k5	MF	2		38615
R885	560	CF			21798
R886	6k2	MF	2		38613
R887	6k2	MF	2		38613
R891	10k	CF			21809
R892	180k	CF			21822
R893	33k	CF			21814
N801	10k	Resistor Network			450452
N802	10k	Resistor Network			450452
N803	4k7	Resistor Network			39225
N804	10k	Resistor Network			450452

CAPACITORS				
C803	220pF	PS	63V	35914
C804	10nF	CE(3)	25V	450548
C805	10nF	CE(3)	25V	450548
C806	10µF	E	25V	32180
C807	10µF	E	25V	32180
C808	100pF	CE(3)	50V	42420
C809	10µF	E	25V	32180
C810	10µF	E	25V	32180
C811	10nF	CE(3)	25V	450548
C812	10µF	E	25V	32180
C813	10nF	CE(3)	25V	450548
C814	10µF	E	25V	32180
C815	10nF	CE(3)	25V	450548
C816	10µF	E	25V	32180
C818	10nF	CE(3)	25V	450548
C819	10nF	CE(3)	25V	450548

OS1400 D.S.O. CIRCUIT (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
C821	1nF	CE(3)			42432
C822	2.2nF	CE(3)			42436
C823	100nF	CE(3)			43498
C824	10nF	CE(3)		25V	450548
C825	10nF	CE(3)		25V	450548
C826	1nF	CE(3)			42432
C829	100pF	CE(3)			42420
C830	5.6pF	CE(3)			42405
C831	100nF	CE(3)			43498
C832	100nF	CE(3)			43498
C833	10nF	CE(3)		25V	450548
C834	100nF	CE(3)			43498
C836	10µF	E		25V	32180
C837	100nF	CE(3)			43498
C838	10µF	E		25V	32180
C841	10nF	CE(3)		25V	450548
C842	10nF	CE(3)		25V	450548
C843	10nF	CE(3)		25V	450548
C844	10nF	CE(3)		25V	450548
C845	10nF	CE(3)		25V	450548
C846	10nF	CE(3)		25V	450548
C847	47pF	CE(3)			42416
C848	10nF	CE(3)		25V	450548
C849	10nF	CE(3)		25V	450548
C850	10nF	CE(3)		25V	450548
C851	10nF	CE(3)		25V	450548
C852	10nF	CE(3)		25V	450548
C853	10nF	CE(3)		25V	450548
C854	47nF	CE(3)			43497
C855	100nF	CE(3)			43498
C856	2.2µF	E		63V	32194
C857	10µF	E		25V	32180
C858	100nF	CE(3)			43498
C859	10nF	CE(3)		25V	450548
C860	100nF	CE(3)			43498
C861	10nF	CE(3)		25V	450548
C862	100nF	CE(3)			43498
C863	10nF	CE(3)		25V	450548
C864	1nF	CE(3)			42432
C865	10nF	CE(3)		25V	450548
C867	470nF	CE(3)		25V	43500
C868	10nF	CE(3)			450548
C869	10nF	CE(3)		25V	450548
DIODES					
D801	2V7	ZENER			33921
D802	2V7	ZENER			33921
D803		ZC2811H			40352
D804		ZC2811H			40352
D805		IN4148			23802
D806		IN4148			23802
D807		OA47			4468
D808		OA47			4468
D809		IN4148			23802
D810		IN4148			23802
D811		IN4148			23802
D812		IN4148			23802
D813		IN4148			23802
D814		IN4148			23802
D815	3V9	ZENER			33925
D816	3V9	ZENER			33925
D817	6V2	ZENER			40045
D818		IN4148			23802
D819	3V9	ZENER			33925
D820	3V9	ZENER			33925
D821	6V2	ZENER			40045
D822		IN4148			23802
D823		OA47			4468
D824		OA47			4468
D825		OA47			4468
D826		OA47			4468
D827		OA47			4468
D828		OA47			4468
D829		OA47			4468
D830		OA47			4468
D831		OA47			4468
D832		OA47			4468
Q801		DUAL FET			44704
Q802		2N5771			38089
Q803		MPS2369			36625
Q804		MPS2369			36625
Q805		MPS2369			36625
Q806		MPS2369			36625
Q807		MPS2369			36625
Q808		2N3906			21533
Q809		2N3906			21533
Q810		2N3906			21533
Q813		MPS2369			36625
Q814		MPS2369			36625
Q815		2N3906			21533
U801		74ALS04			451301
U802		74ALS00			451299
U803		74ALS00			451299
U804		74LS00			36730
U805		74LS10			36867
U806		74ALS74			451308
U807		74LS162			450681
U808		4081			37694
U809		74LS00			36730
U812		4011			34953
U813		74LS51			43676
U814		4044			44024
U815		TCD1001J			450682
U816		74LS374			43386
U817		HM6116P-3			450683
U818		DAC10			451264
U819		74C374			451266
U820		DAC08			450686
U821		4053			41891
U822		4049			36200

OS1400 D.S.O. CIRCUIT (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
DIODES (Cont.)					
U823		4011			34953
U824		74C00			451282
U825		TL082			451262
U826		4049			36200
U827		LF347CN			450908
U828		74LS123			41084
U829		74ALS04			451301
U831		MT7009-1			450600
U832		74LS26			44362
U833		4011			34953
U834					
U835		74ALS74			451308
U836		74C74			451290
U837		74C00			451282
U838		74C74			451290
TRANSISTORS					
T801					A4/450687
MISCELLANEOUS					
XL801		CRYSTAL 20MHz			450688
		SKHH			450771
		SKJJ			450771
		SKKK			38001

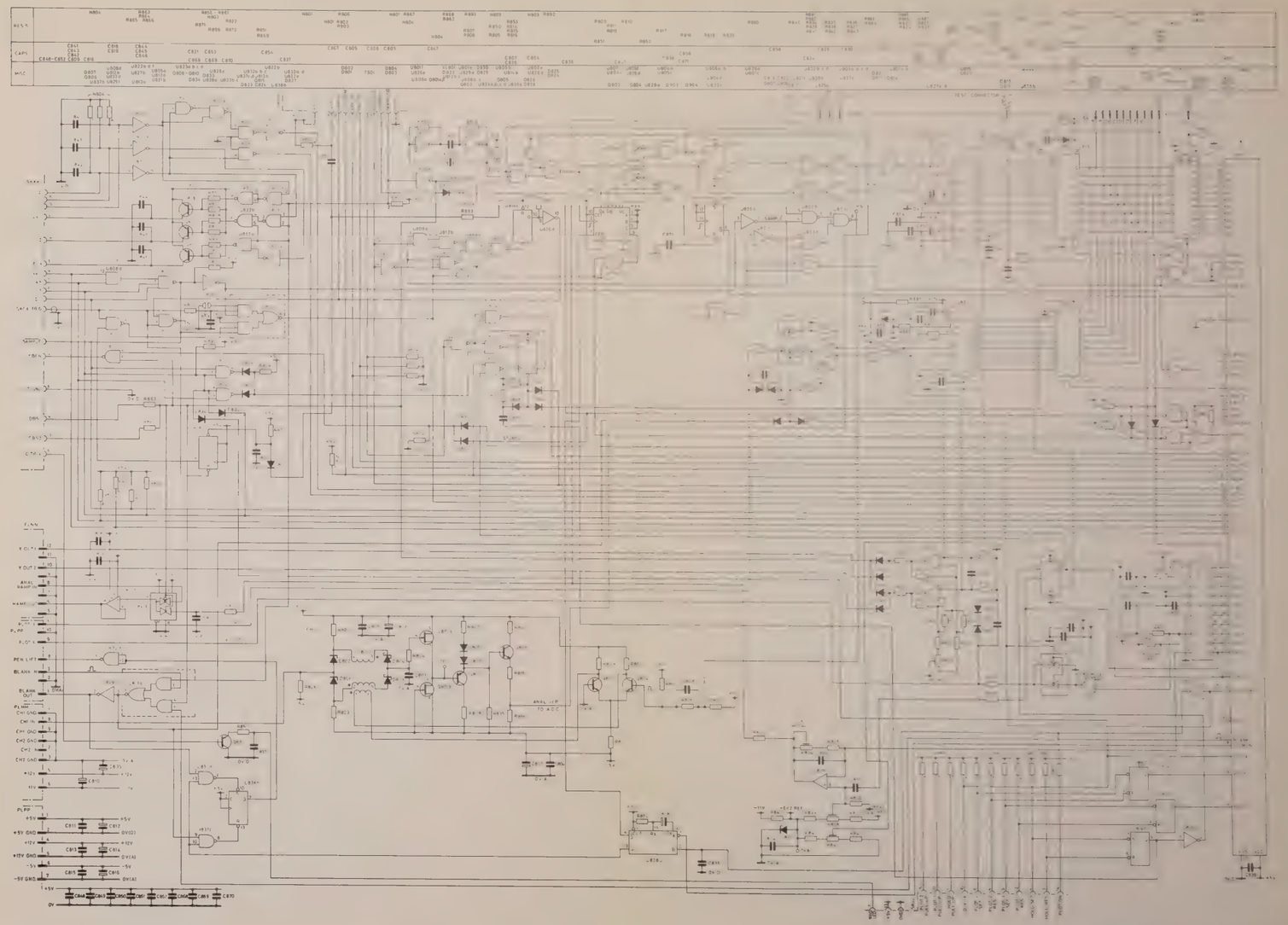


Fig. 10 Digital Storage Circuit Diagram

OS1400 POWER SUPPLY AND CRT

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R701	1k	CF			21799
R702	680	CF			28723
R703	10k	CF		1W	2882
R704	22k	CF			21812
R705	5k6	CF			21806
R706	470	CF			21797
R707	8k2	CF			21808
R708	220k	PCP			36270
R710	2k2	CF			21802
R713	470k	PCP			36271
R714	1M	CF		½W	18588
R715	680k	CF			31839
R716	33M	MG	5	½W	43008
R717	33M	MG	5	½W	43008
R718	22k	CF	10		3433
R719	18k	CF		½W	18565
R721	180	CF		½W	18541
R722	1k	CF			21799
R723	2k2	CF			21802
R724	5k6	CF			21806
R725	47k	PCP			38261
R726	33k	MF	2		38630
R727	150	CF			28719
R728	68	CF			28716
R729	680	CF			28723
R730	1k	CF			21799
R731	10k	MF	2		38618
R732	47k	CF			21815
R733	22k	CF	10		3433
R734	68	CF	A.O.T.		28716
R735	1k5	CF			21801
R736	1k	CF			21799
R737	10k	PCP			44959
R738	180	MF	2		38576
R739	47	CF		½W	18534
R741	5k6	CC	5		2363
R742	220k	MF	2		38650
R743	33M	MG	5	½W	43008
R744	1M	CP			A4/44460
R745	10k	CP	WITH S1		A4/44461
R746	82k	CF			21818
R747	120k	CF			21820
R748	100k	CF			21819
RN720		RESISTOR NETWORK			A3/44608
DIODES					
D701		IN4148			23802
D702		IN4148			23802
D704		L.E.D.			43847
D705		BAX17			402022
D706	150V	ZENER			37559
D708		IN4148			23802
D709	200V	ZENER			40052
D711	9V1	ZENER			33934
D712	5V1	ZENER			33928
D713		IN4148			23802
D714		IN4148			23802
D715	200V	ZENER			40052
D716	200V	ZENER			40052
D717	200V	ZENER			40052
D718	12kV				44550
D719	12kV				44550
D720		IN4148			23802
D721		BAX17			402022
D722		IN4004			450266
D723		IN4004			450266
D724		IN4004			450266
D725		IN4004			450266
D726		IN4004			450266
D727		IN4004			450266
D728		IN4004			450266
D729		IN4004			450266
D730	200V	ZENER			40052
MISCELLANEOUS					
V1		MULLARD 56825GY NORMAL VERSION			44932
T1					451429
SKG					37293
SKH					37293
PLM					44960
F701	125mA				450551

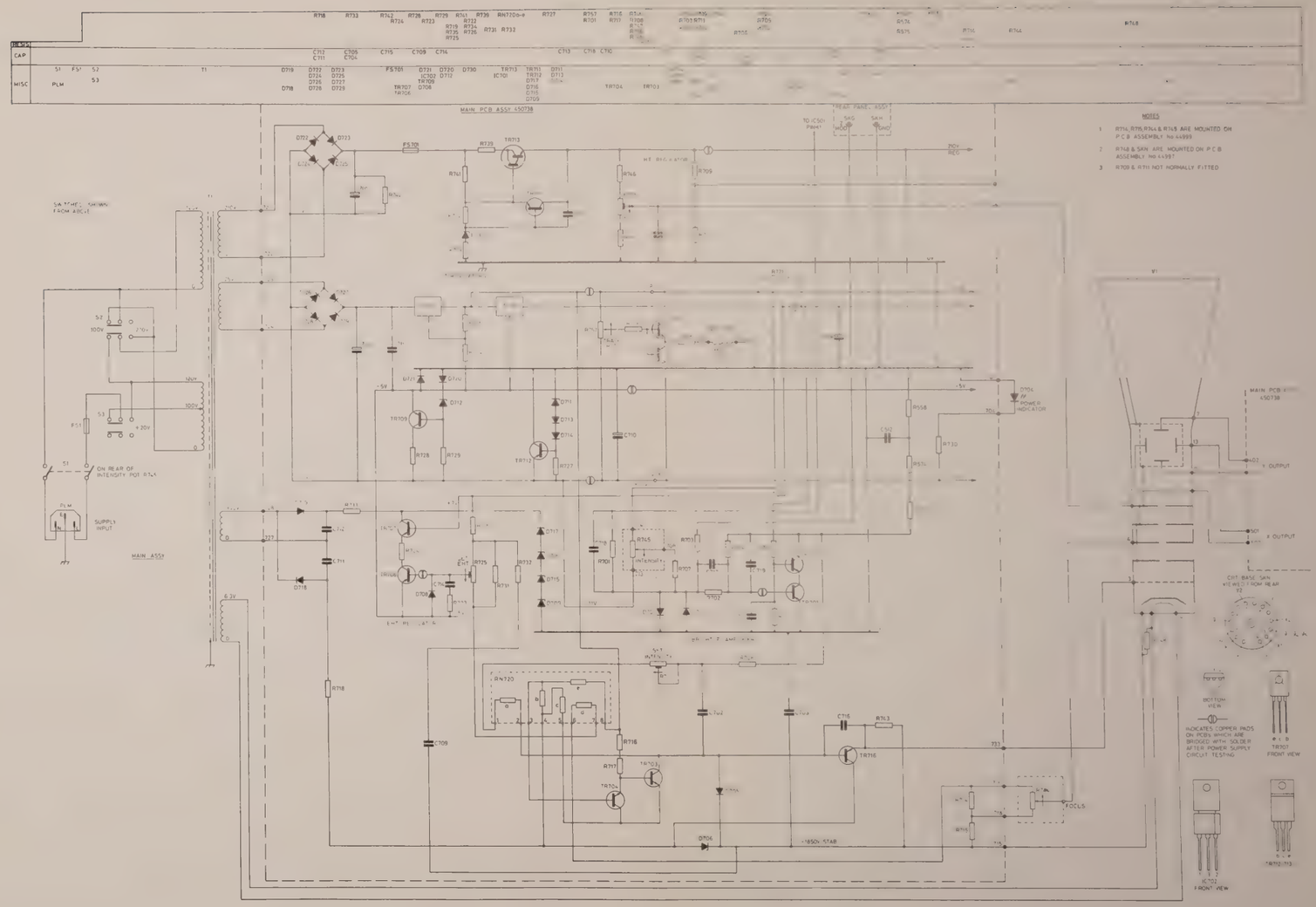


Fig. 11 Power Supply and CRT Circuit Diagram

OS1400 AUXILARY POWER SUPPLY

Ref	Value	Description	Tol %±	Rating	Part No	Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS											
C1201	4700µF	E		16V	450795	D1203		IN4003			23462
C1202	10nF	CE(3)		25V	450548	D1204		IN4003			23462
C1203	2.2µF	T		35V	35930	D1205		IN4003			23462
C1204	2200µF	E		25V	450631	D1206		IN4003			23462
C1205	10nF	CE(3)		25V	450548	D1207		IN4003			23462
C1206	2.2µF	T		35V	35930	D1208		IN4003			23462
C1207	3300µF	E		16V	44517	D1209		IN4003			23463
C1208	10nF	CE(3)		25V	450548	D1210		IN4003			23463
C1209	2.2µF	T		35V	35930	D1211		IN4003			23463
						D1212		IN4003			23463
DIODES						U1201		7805			36176
D1201		IN4003			23462	U1202		7812			36178
D1202		IN4003			23462	U1203		7905			36182

CAPS	C1201 C1207 C1208 C1209
MISC	T1 D1201 – D1212 U1201

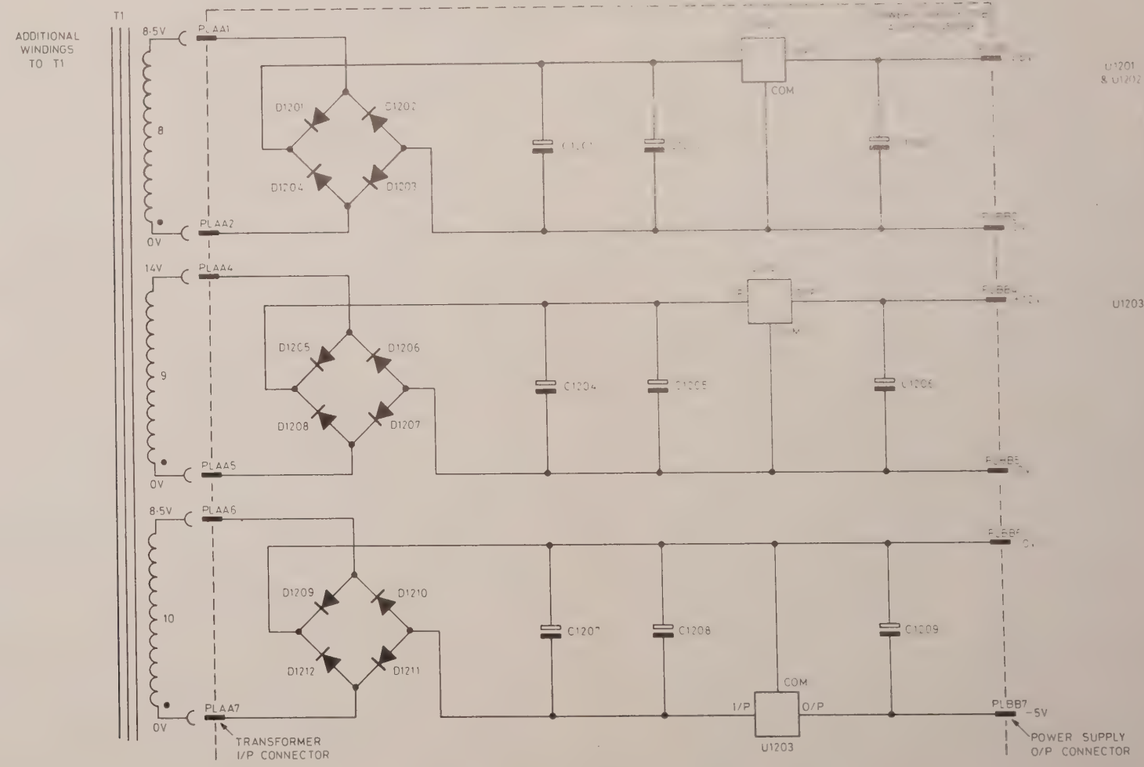


Fig. 11 Power *Fig. 12 Auxilliary View*

Ref	Description	Part No
1	Frame/Panel Moulding	451068
2	Panel Rear	451595
3	Support Side (Long)	450730
4	Side Support (Short)	450043
5	Coverlay Focus/Brill	450754
6	Coverlay Pushbuttons	450996
7	Clamp C.R.T. (Moulding)	450009
8	Base C.R.T. (Moulding)	450008
9	Cover Rear (Moulding)	44969
10	Holder Fuse	40068
11	Connector Supply	44960
12	Earth Spring	44984
13	Graticule Blue	44964
14	Panel Front	44478
15	Coverlay	450991
16	Screen Timebase	44972
17	Screen Attenuator	44973
18	Screen B.N.C. Sockets	450089
19	Heatsink	450648
20	Heatsink (Aux Power Supply)	450752
21	Case Bottom	450768
22	Case Top	450769
23	Button Handle	36681
24	Spindle Moulded	44470
25	Cover Handle	44471
26	Base Handle	44472
27	Foot	36329
28	Spring	44568
29	Handle Assy	44469
30	Washer C.R.T.	44963
31	Knob – Pushbutton	38407
32	Knob 10mm 'D' Type	402009
33	Knob 15mm 'D' Winged	402010
34	Knob R2–234	40408
35	Knob R4–454 (21mm)	40410
36	Cap W1–208	44957
37	Cap W1–400	44958
38	Cap W1–300	44959
39	'POP' Rivet	450690
40	Rivet .2" Long	12862
41	Rivet .29" Long	29426
42	Bezel	43256
43	Grommet	382
44	Terminal	24159
45	Fuse 500mA	33685
46	Fuse 250mA	33684
47	Screw M4 x 12 C'sk Hd.	33077
48	Screw M4 x 8 Pan Hd.	33044
49	Screw M4 x 10 Pan Hd.	33045
50	Screw M3 x 8 Pan Hd.	33038
51	Nut M3 Sq.	41407
52	Nut M3	33023
53	Washer M3 Wavey	33016
54	Washer M4 Wavey	33017

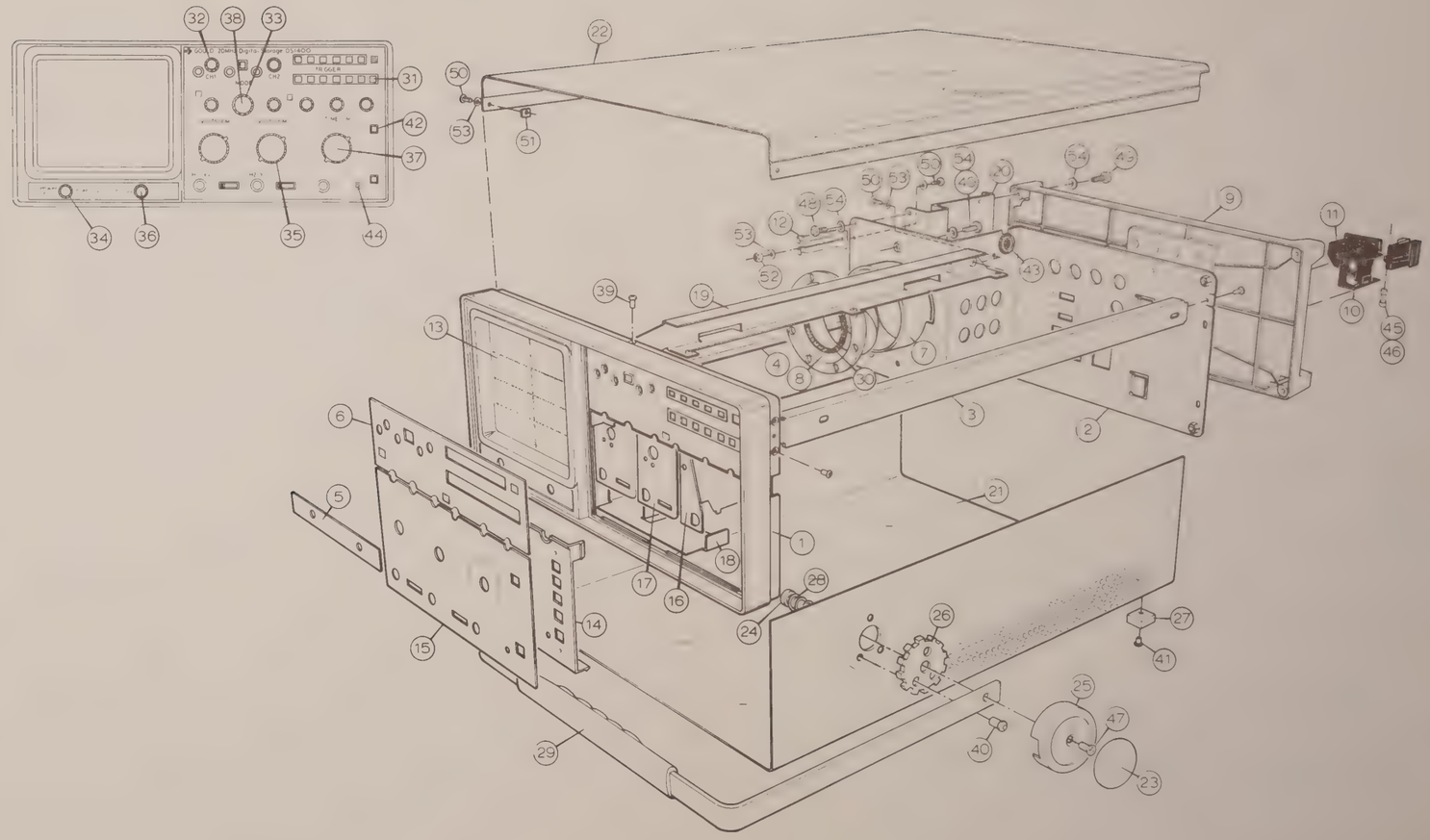


Fig. 13 Mechanical View Circuit Diagram

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of two years from its delivery to the purchaser, covering faulty workmanship and replacement of defective parts other than cathode ray tubes and batteries (where fitted). Cathode ray tubes are subject to the manufacturers guarantee. This assumes fair wear and tear and usage in the specified environment and does not cover routine recalibrations and mechanical adjustments.

We maintain comprehensive after sales facilities and the instrument should be returned to our factory for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the instrument was supplied and shipped with transportation charges prepaid. We accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired the repair will be put in hand without delay and charged unless other instructions are received.

Our Sales, Service and Engineering Departments are ready to assist you at all times.

The Service Department can provide maintenance and repair information by telephone or letter, if required.

Note: Please check fuses before returning instruments for service and ensure that any 13 Amp mains plugs fitted are removed. To prevent possible transit damage, we regret that mains plugs cannot be returned.

Service Dept.,
Roebuck Road,
Hainault,
Essex,
IG6 3UE

Tel: 01-500 1000
Telex: 263785
Telegrams: Attenuate Ilford

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